

C74-6502 PCB Patch Guide (v1.0 Boards)

The following patches were applied to the C74-6502 V1.0 prototype boards during debugging. Patches are divided into three categories:

- **Mandatory** patches that need to be made in order for the CPU to function properly,
- **Recommended** patches that are not strictly required but should be made under most circumstances,
- **Optional** patches which provide compatibility with specific features and may be desirable.

Each patch includes a “rationale” which provides helpful information to determine whether a given patch should be applied or not.

Patches list specific jumper connections that must be made as follows:

Card X: from_ICName.pin_number (PAD/LIFT) —> to_ICName.pin_number (PAD/LIFT)

Where:

- “Card X” refers to the Card in which the patch should be made. A diagram of the relevant card (top or bottom view as appropriate) with the relevant ICs highlighted accompanies patch instructions. Refer to the diagram to locate the ICs involved in the patch. See NOTE below.
- “From_ICName._pin_number”, “to_ICName.pin_number” refer to specific pins of named ICs that must be connected together via jumpers
- “(LIFT)”, if present, indicates that the pin should be lifted off its pad before the jumper connected to it
- “(PAD)”, if present, indicates that the pin should be lifted off its pad and the jumper connected to the pad only
- If neither “(LIFT)” or “(PAD)” are shown, the jumper should be connected to pin and pad together
- “ICName,pin (LIFT)” on its own without a following “—>” indicates that the pin should be lifted off its pad. A subsequent instruction will indicate whether the jumper should be connected to the pad or pin as appropriate.

Annotated schematics which reflect these patches can be found on: <https://c74project.com/c74-6502-internals/>

NOTE: the IC numbers on the silkscreens of Cards B and C do NOT correspond to those shown on the schematics. In the instructions below, the schematic IC numbers are used. Corresponding silkscreen numbers also are shown in square brackets next to the instruction in which they are used. Use the location of the IC on the board, as well as its silkscreen reference, to verify the right IC for each patch.

In some cases, connections must be made to specific inter-card connector pins, e.g., “X5.3” refers to inter-card connector 5, pin 3. The inter-card connectors are located around the perimeter of each card. The specific pin to be patched to is highlighted in the diagram which accompanies each patch.

1. 6510 PORT — REVERSED PINS ON PBAD, INVERTED POLARITY OF /BE

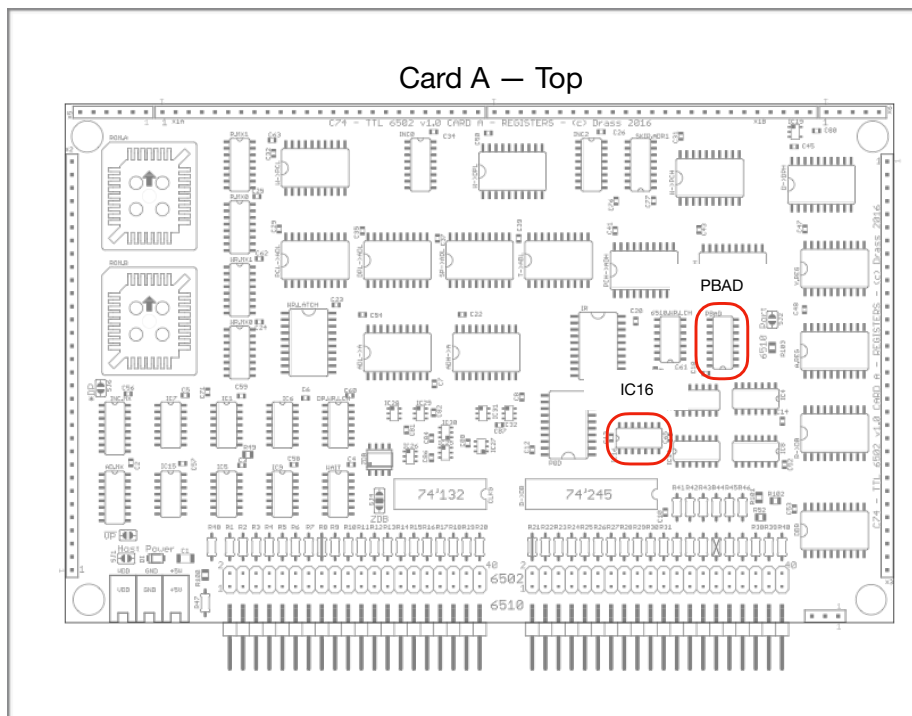
Description: The v1.0 boards had certain pins reversed on the PBAD IC (part of the 6510 port). This patch makes the correct connections on PBAD, and skips the inverter on PBAD.5 to have the right polarity.

Category: Mandatory

Rationale: This patch must be made in order for the 6510 port to work properly

Patch 1:

- Card A: PBAD.11 (LIFT) —> PBAD.10 (PAD)
- Card A: PBAD.10 (LIFT) —> PBAD.11 (PAD)
- Card A: PBAD.7 (LIFT) —> PBAD.9 (PAD)
- Card A: PBAD.9 (LIFT) —> PBAD.7 (PAD)
- Card A: IC16.3 (LIFT)
- Card A: IC16.3 (PAD) —> PBAD.5 (LIFT)



2. T->R INPUTS PINS REVERSED

Description: The v1.0 boards had pins on the T->R buffer reversed. This patch corrects these connections.

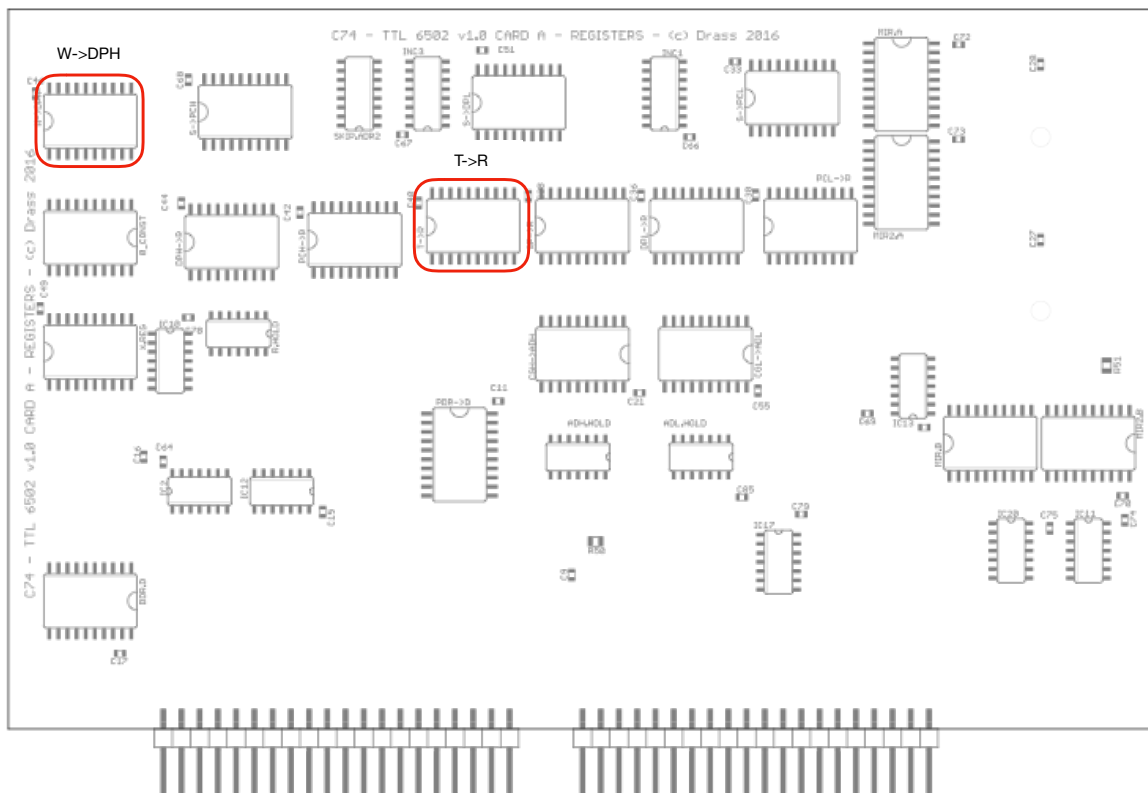
Category: Mandatory

Rationale: This patch must be made for the CPU to work properly.

Patch 2: Correct inputs of T->R

- Card A: T->R.7 (PAD) → T->R.6 (LIFT)
- Card A: T->R.8 (PAD) → T->R.7 (LIFT)
- Card A: T->R.9 (PAD) → T->R.8 (LIFT)
- Card A: W->DPH.9 → T->R.9 (LIFT)

Card A — Bottom



2A. S->PCH OUTPUT PINS REVERSED

Description: The original schematics had pins on the S->PCH buffer reversed. This patch corrects there connections.

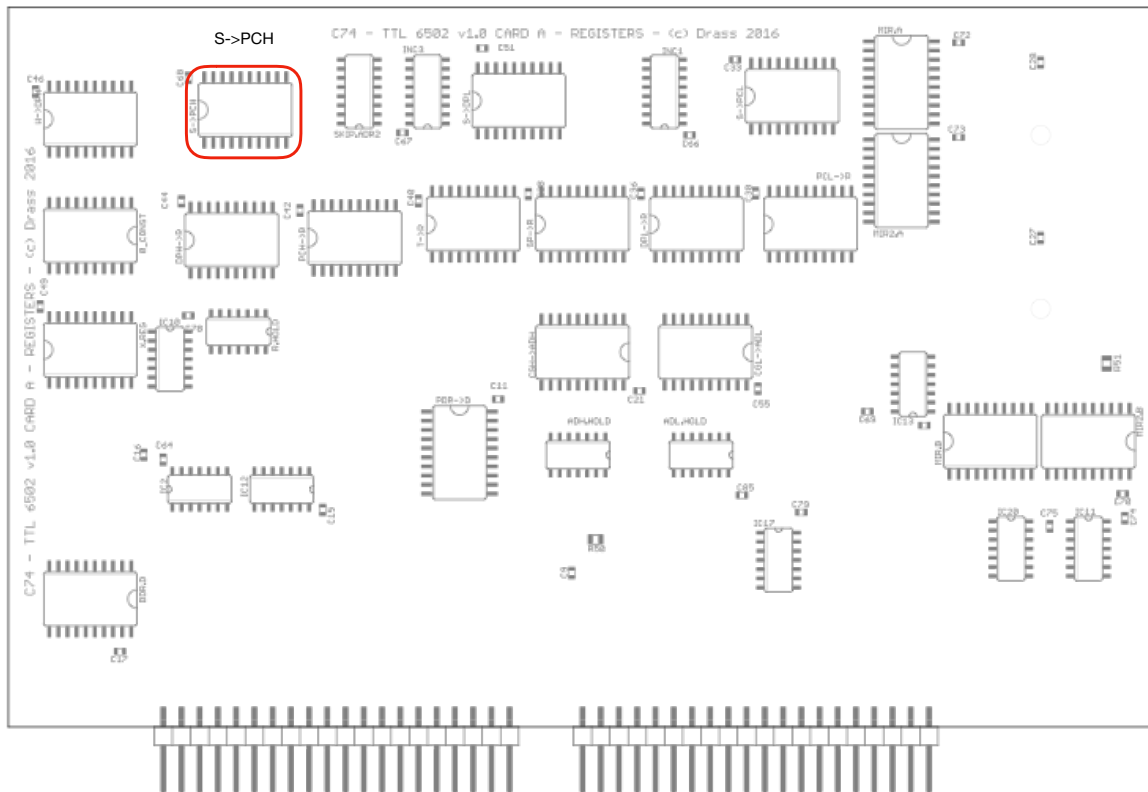
Category: Mandatory

Rationale: This patch must be made for the CPU to work properly

Patch 2A: Correct outputs of S->PCH

- Card A: S->PCH.11 (LIFT) -> S->PCH.18 (PAD)
- Card A: S->PCH.12 (LIFT) -> S->PCH.17 (PAD)
- Card A: S->PCH.13 (LIFT) -> S->PCH.16 (PAD)
- Card A: S->PCH.14 (LIFT) -> S->PCH.15 (PAD)
- Card A: S->PCH.15 (LIFT) -> S->PCH.14 (PAD)
- Card A: S->PCH.16 (LIFT) -> S->PCH.13 (PAD)
- Card A: S->PCH.17 (LIFT) -> S->PCH.12 (PAD)
- Card A: S->PCH.18 (LIFT) -> S->PCH.11 (PAD)

Card A — Bottom



3. 65C02 NOP1 OPCODES

Description: NOP1 opcodes are single cycle NOPs present in the 65C02 instruction set. A bug in the sequencer logic prevented these from being executed properly. Fixing this bug also simplified the sequencer logic and microcode. For that reason, this patch is required for all instruction sets, and must be made for the CPU to work properly. The patch involves jumpers on both the top and bottom of Card B.

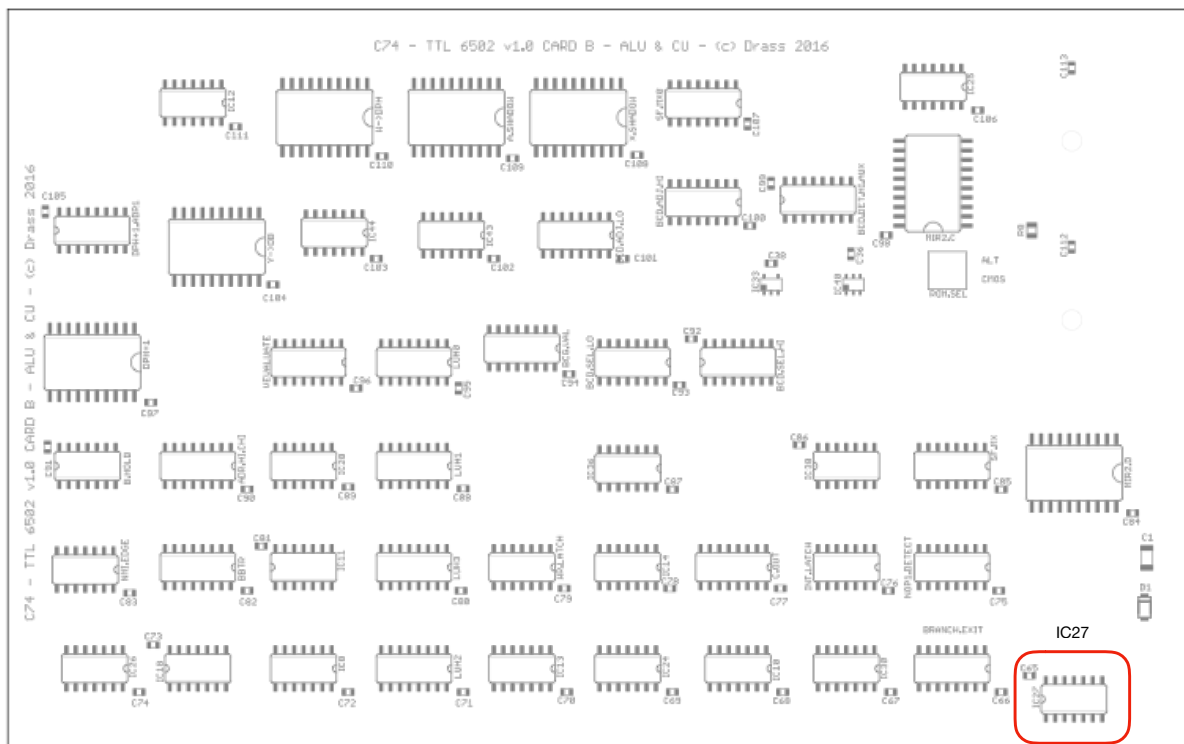
Category: Mandatory

Rationale: This patch must be made for the CPU to work properly.

Patch 3: part 1

- Card B: IC27.14 → IC27.1 (LIFT) [IC27 = silkscreen IC50]

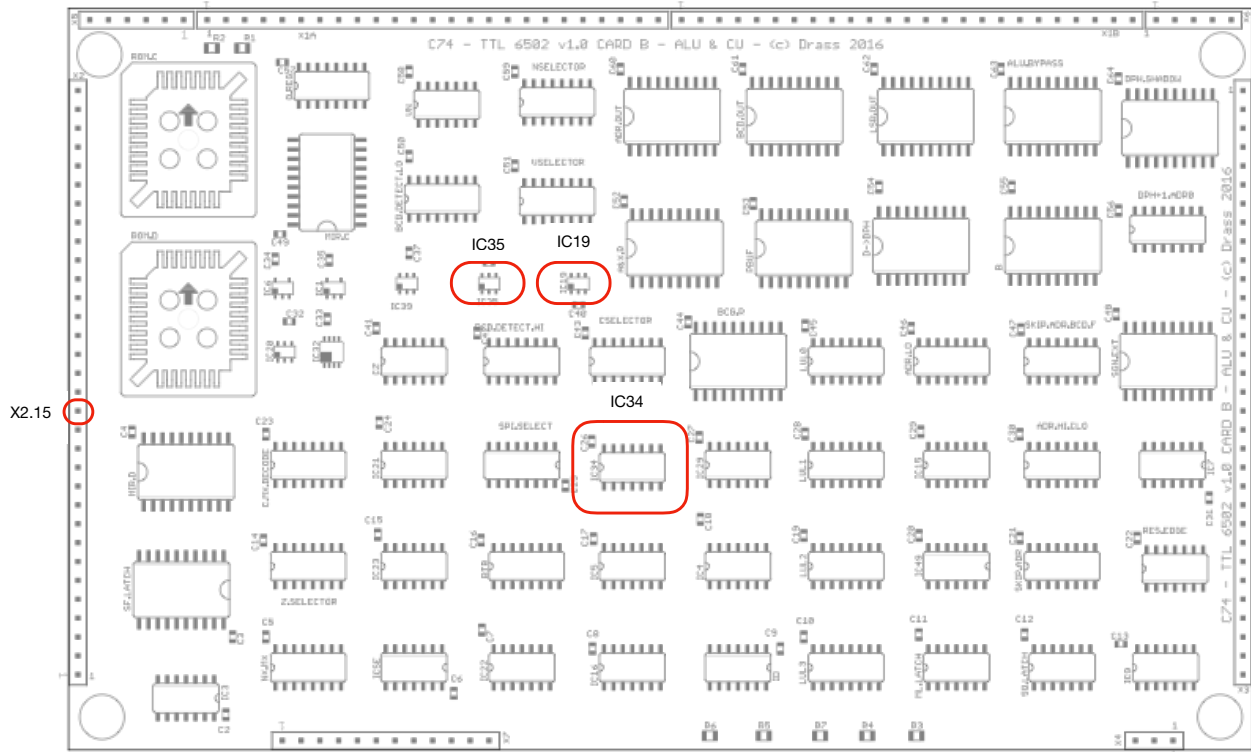
Card B — Bottom



Patch 3: part 2

- Card B: X2.15 → IC34.11 (LIFT) [IC34 = silkscreen IC36]
- Card B: IC34.10 → IC19.3 (LIFT) [IC19 = silkscreen IC53]
- Card B: IC35.3 → IC35.1 (LIFT) [IC35 = silkscreen IC57]

Card B – Top



4. R/W TAKES TOO LONG BEYOND 16MHZ

Description: Speed tests revealed that the CPU takes too long to generate R/W when operating above 16MHz. This patch reduces the propagation delay for the R/W signal by taking one gate out of the path.

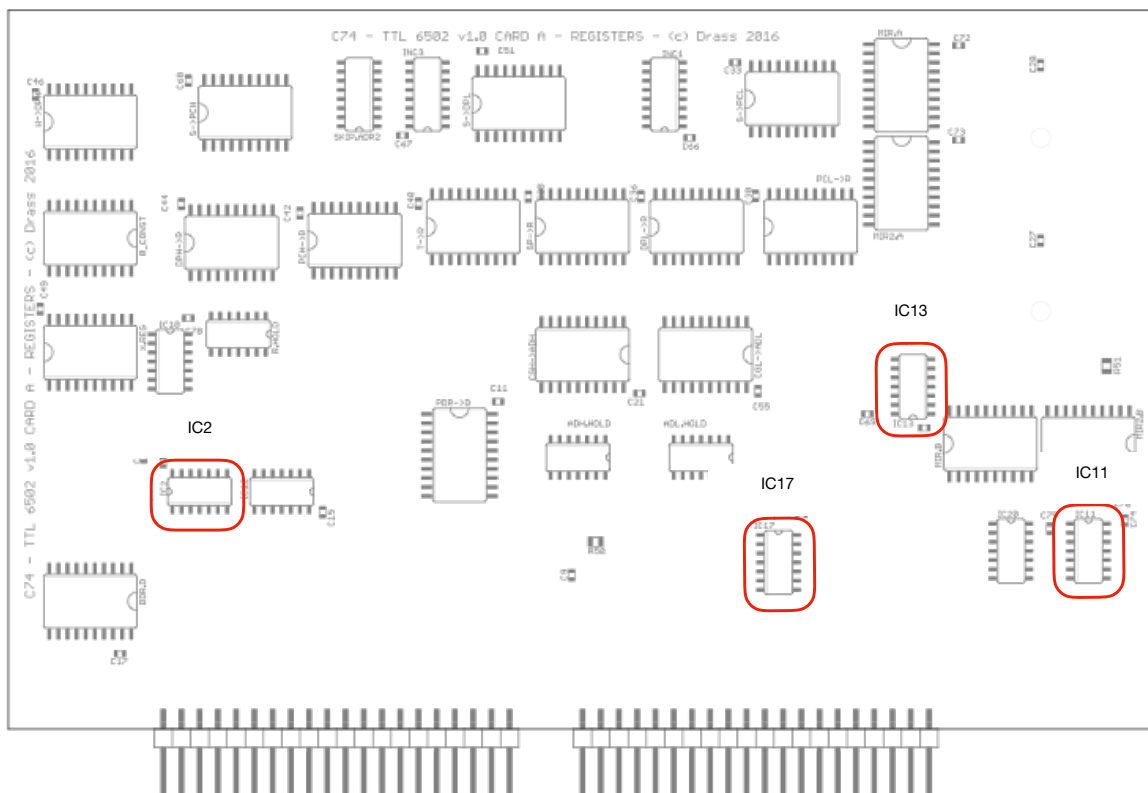
Category: Recommended

Rationale: This patch should be applied if operation at clock-rates above 16MHz is planned.

Patch 4:

- Card A: IC11.10 → IC17.9 (LIFT)
- Card A: IC13.3 → IC17.10 (LIFT)
- Card A: IC17.8 → IC2.12
- Card A: IC5.10 (LIFT)

Card A — Bottom



5. COMPATIBILITY WITH BUS SHARING SCHEMES

Description: The C74-6502 was designed to drive the bus during Phase 1 only. This is in order to avoid transient bus collisions at high speeds. Unfortunately, this bus scheme is not compatible with systems where the CPU shares control of the bus with other peripherals (such as on the Commodore 64 and others). This patch will cause the CPU to drive the bus during Phase 2 as well as Phase 1. This will lead to short transient collisions on the bus during state transitions, but these are benign and can be safely ignored.

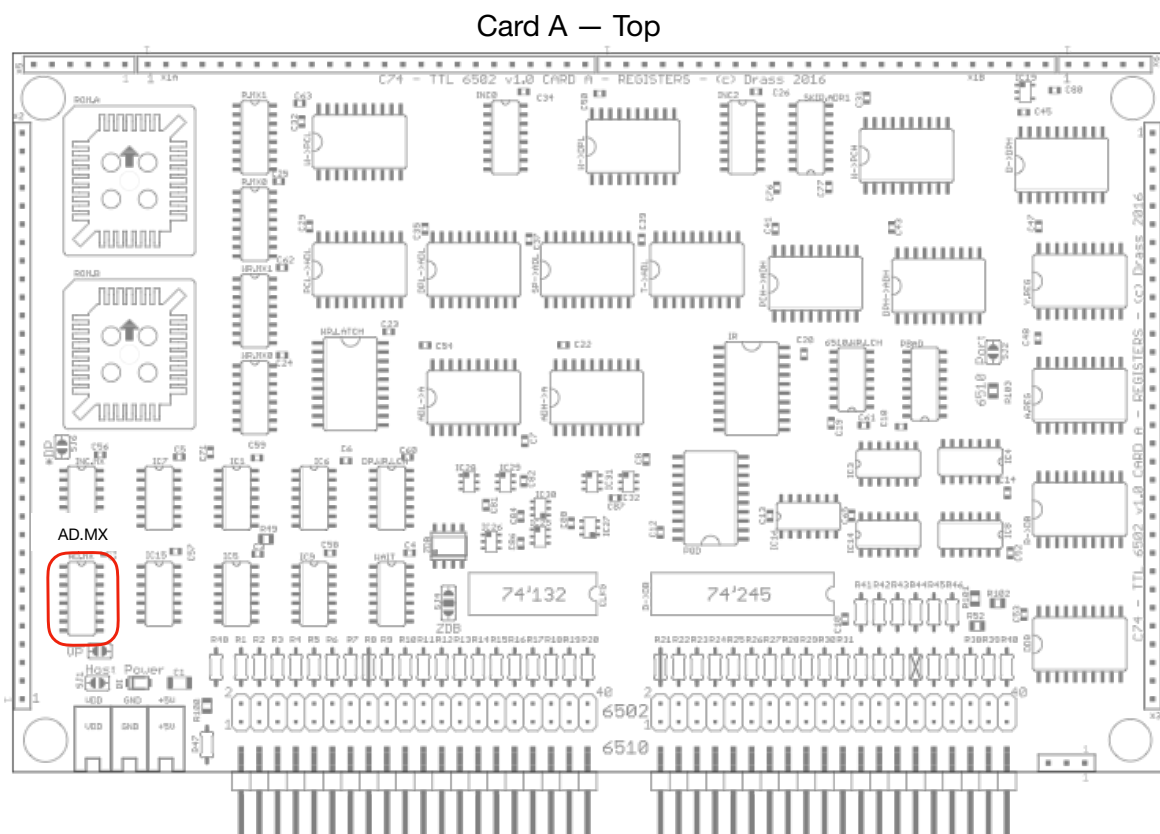
Category: Recommended

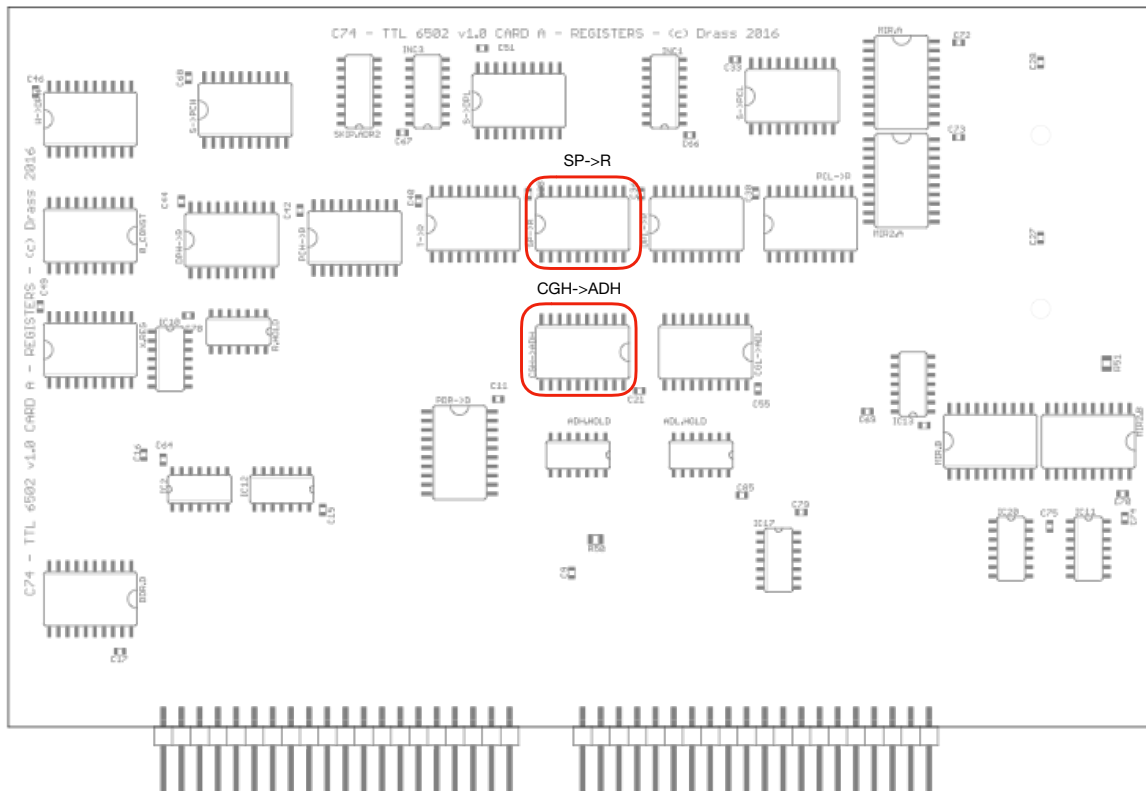
Rationale: Required for operation in machines that implement bus sharing schemes (e.g. Commodore 64)

Patch 5:

- Card A: AD.MX.5 → AD.MX.4 (LIFT)
- Card A: SP→R.10 → CGH→ADH.1 (LIFT)

Note: Need to test whether applying this patch inhibits operation at the highest clock-rates. If so, consider replacing ADL.A and ADH.A 74CBT3245s with 74AC541s.





6. RDY TAKES EFFECT ONE CYCLE TOO LATE AND RDY NMOS 6502 COMPATIBILITY

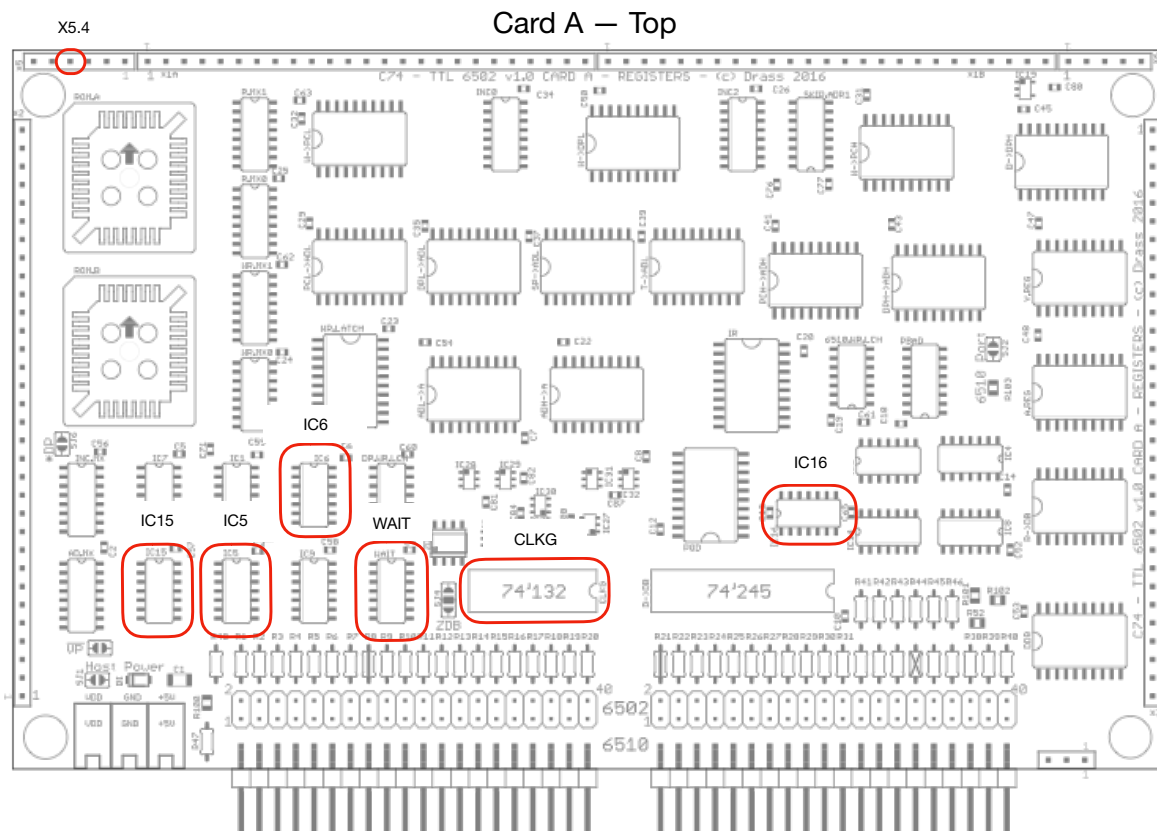
Description: The RDY signal is meant to pause the CPU during Phase 2 of the cycle in which it is detected. Instead, the TTL CPU was pausing during Phase 1 of the following cycle. In addition, RDY should not pause the CPU on reads when emulating the NMOS 6502 but should do so for the 65C02. This patch will cause the RDY to correctly pause the CPU during Phase 1, and its behaviour will adjust automatically based on the active instruction-set.

Category: Recommended for compatibility with timing-sensitive applications and any peripherals which require wait-states.

Rationale: This came up in testing when accessing devices that require wait-states, as well as on the Commodore 64 where timing sensitive applications expect strict adherence to the NMOS 6502 behaviour.

Patch 6:

- Card A: CLKG.4 → CLKG.5 (LIFT)
- Card A: CLKG.5 (SOCKET) → WAIT.2 (LIFT)
- Card A: CLKG.6 → IC6.9 (LIFT)
- Card A: IC6.11 → IC6.10 (LIFT)
- Card A: X5.4 → IC16.3 (LIFT)
- Card A: IC16.4 → IC6.12 (LIFT)
- Card A: IC15.12 → IC6.13 (LIFT)
- Card A: IC6.8 → WAIT.10 (LIFT)
- Card A: WAIT.4 → WAIT.1 (LIFT)
- Card A: WAIT.6 (LIFT)
- Card A: WAIT.5 → WAIT.6 (PAD)
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7. NMOS 6502 MODIFY CYCLE WRITE

Description: The NMOS 6502 performs a Read-Write-Write sequence for RMW instructions (INC, DEC, ASL, etc.). The C74-6502 was designed to duplicate the 65C02 behaviour, which is Read-Read-Write. This patch will cause a Write to be performed during the Modify (middle) cycle when the NMOS 6502 instruction-set is selected.

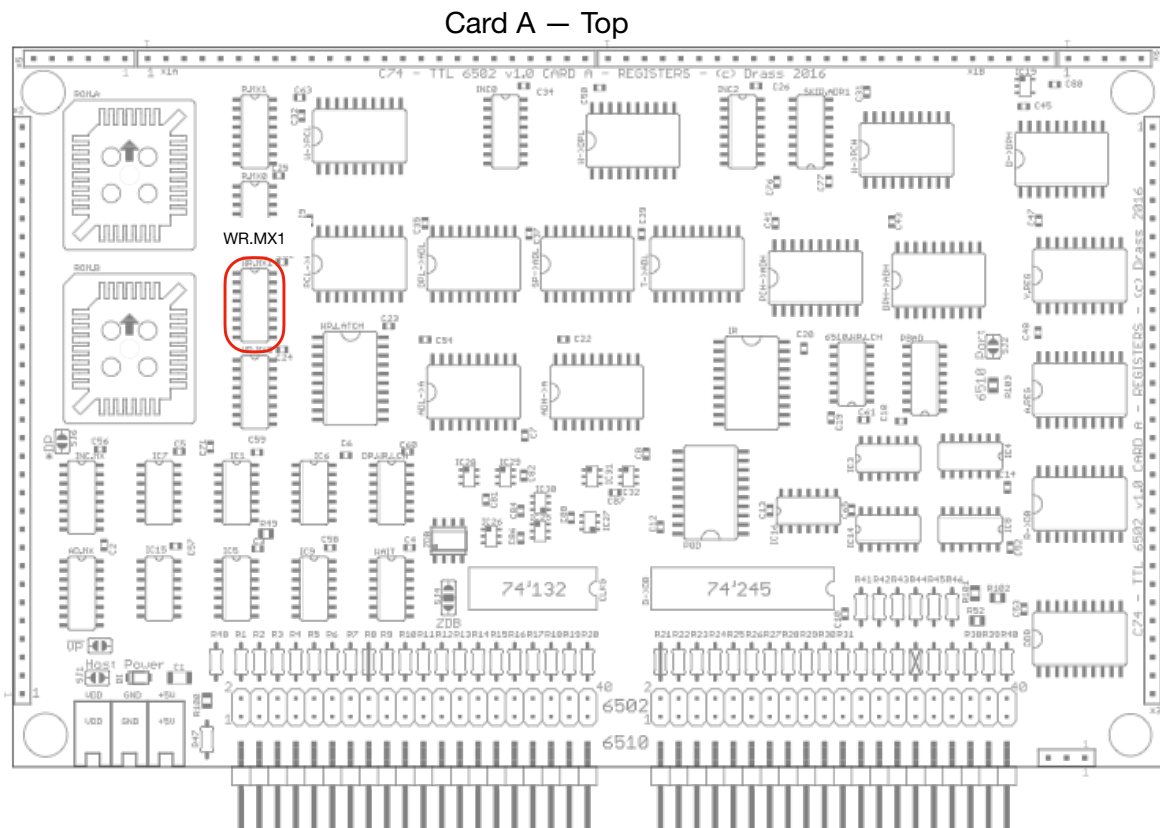
Category: Recommended

Rationale: Several Commodore 64 games were found to rely on a Modify-Cycle-Write to clear the raster interrupt on the VICII chip. This is fairly common practise on more advanced games. Most 65C02 systems will work when the NMOS Modify-Cycle-Write behaviour is in effect. However, the reverse is not true. It is therefore recommended that the patch be made unless operation on NMOS 6502 systems is not planned.

WARNING: This patch disables "H+1" undocumented opcodes (see C74-6502 datasheet p. 21). These opcodes are classified as "unstable", meaning that they produce different results on different 6502 systems. Their use is extremely rare. The C74-6502 implementation is detailed in the datasheet (Appendix F). They are not supported at clock-rates above 14MHz.

Patch 7: Part 1

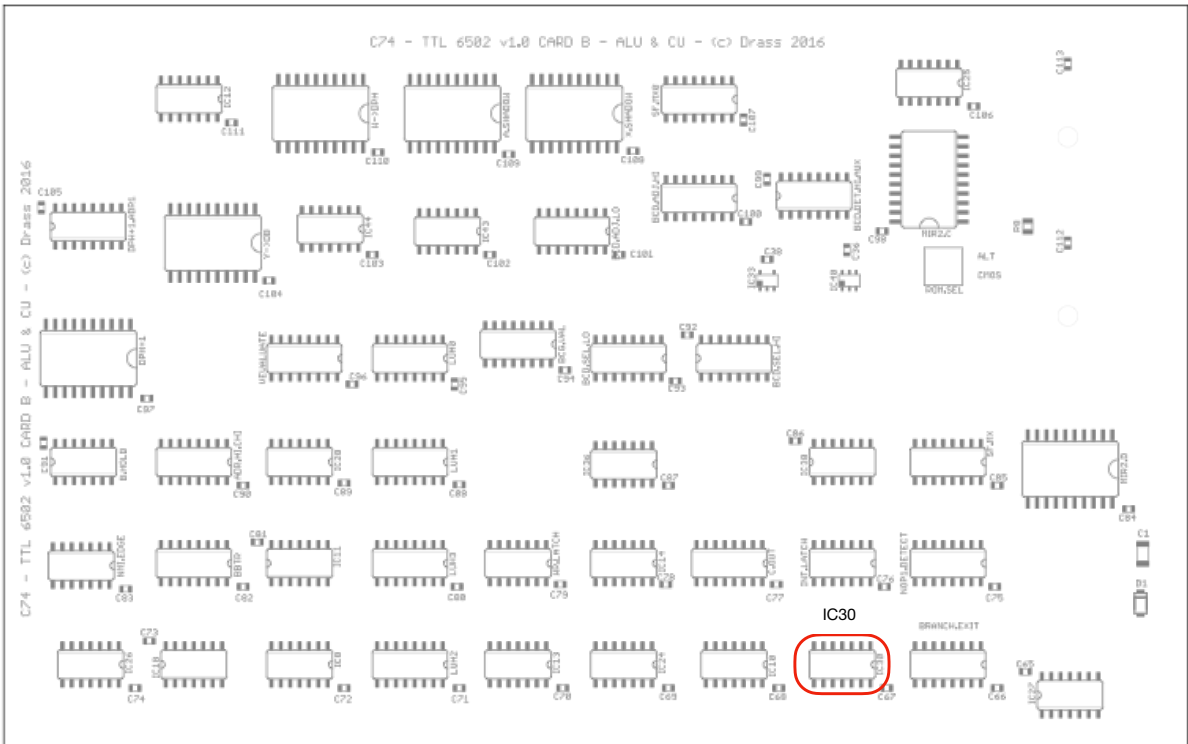
- Card A: WR.MX1.9 (LIFT)



- Card B: IC34.2 (LIFT) [IC34 = silkscreen IC36]
- Card B: IC34.14 → IC34.2 (PAD)
- Card B: IC4.10 → IC30.9 (LIFT) [IC4 = silkscreen IC42]
- Card B: ML.LATCH.5 → IC30.10 (LIFT) [IC30 = silkscreen IC61]
- Card B: IC30.8 → IC34.1 (NO NEED TO LIFT)



Card B — Bottom



8. DEAD-CYCLE — NMOS VS. CMOS COMPATIBLE BEHAVIOUR

Description: The NMOS 6502 produces partial addresses on the bus during address calculation. This was changed on the 65C02, which leaves in place the Previous Bus Address in those situations. This patch enables the “*DP” jumper to select between these two behaviours, leaving the jumper open for NMOS compatible operation, and closing it for CMOS operation.

Category: Optional

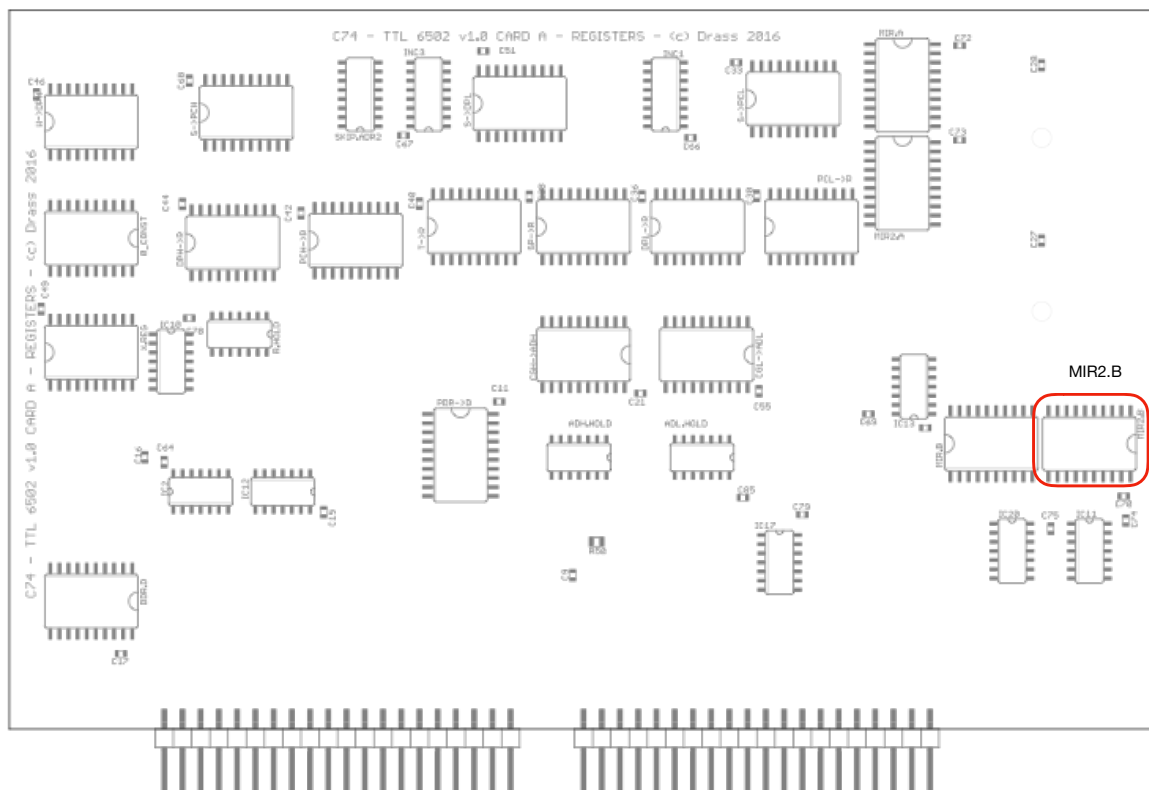
Rationale: Although this is rare, some software on NMOS 6502 systems relies on partial addresses reads during the dead-cycle. This patch is optional. It should be made if strict compatibility with NMOS 6502 is desired. Once applied, close the *DP jumper for CMOS compatibility, and leave it open for NMOS compatibility.

WARNING: This patch requires that ADL.A and ADL.H be replaced with 74AC245s (rather than 74CBT3245s) when operating as a 65C02 in systems which implement a bus sharing scheme (i.e., where the CPU does not have complete control of the address bus).

Patch: Part 1

- Card A: MIR2.B.3 —> MIR2.B.6 (LIFT)
- Card A: MIR2.B.6 (PAD) —> MIR2.B.7 (LIFT)

Card A — Bottom



9. NMI INCORRECTLY INTERRUPTS IRQ

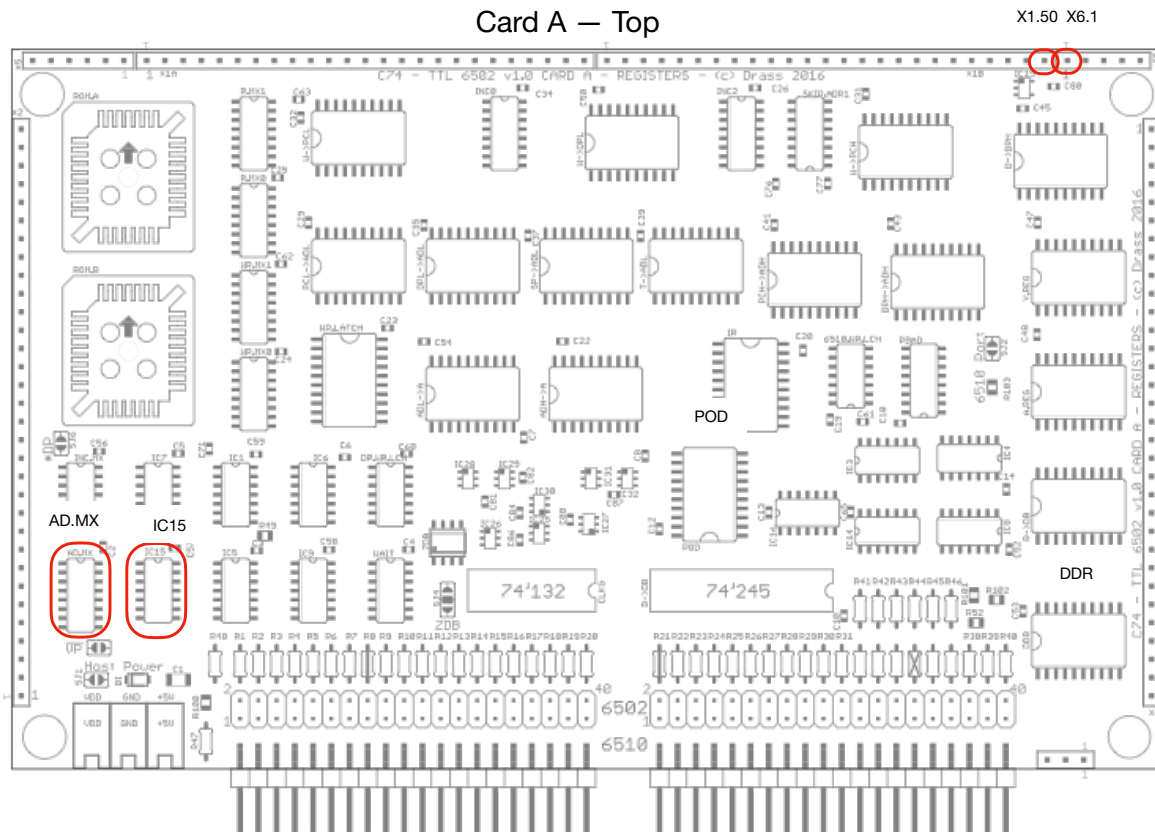
Description: This patch fixes a bug where the CPU will loose an IRQ if an NMI happens to arrive just as the IRQ vector is being fetched by the CPU.

Category: Recommended

Rationale: This bug caused problems for a couple of Commodore 64 games which rely on strict processing of IRQs and also have frequent NMIs occurring. The patch is recommended for strict compatibility with NMOS 6502.

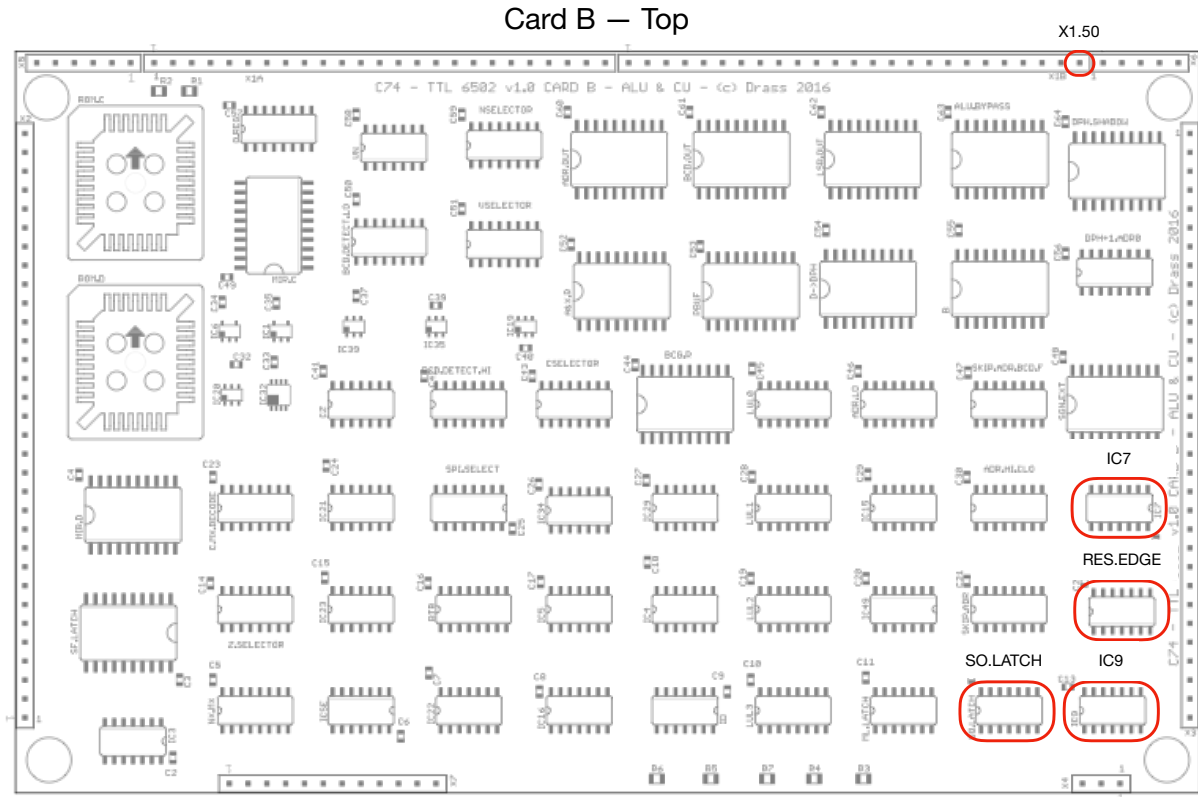
Patch 9: Part 1

- Card A: AD.MX.7 → X1.50
- Card A: IC15.1 → IC15.13 (LIFT)
- Card A: X6.1 → POD.1 (LIFT) → DDR.1



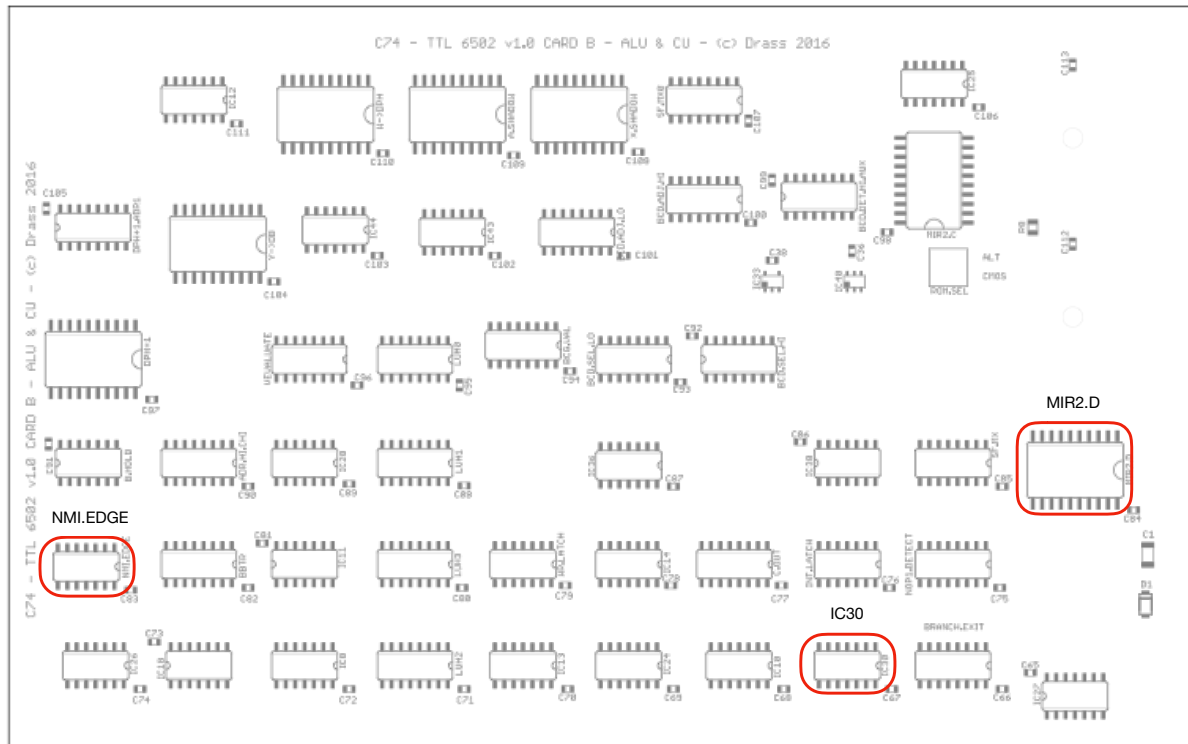
Patch 9: Part 2

- Card B: X1.50 → SO.LATCH.10 (LIFT)
- Card B: IC9.8 → SO.LATCH.11 (LIFT) [IC9 = silkscreen IC40]
- Card B: SO.LATCH.14 → SO.LATCH.13 (LIFT)
- Card B: RES.EDGE.6 (LIFT) → RES.EDGE.11 (LIFT)



- Card B: SO.LATCH.8 → IC30.13 (LIFT) [IC30 = silkscreen IC61]
- Card B: MIR2.D.11 → IC30.12 (LIFT)
- Card B: IC30.11 → NMI.3 (LIFT)

Card B — Bottom



10. WIRING MISTAKES ON K24 CARD C

Description: Mis-wirings on the K24 Card C

Category: Mandatory

Rationale: Required

Patch 10:

- Card C: WR.MX.5 —> WR.MX.4 (LIFT)
- Card C: ROME.31 —> X5.3

Interward Connector X6 pins reversed. Pin 1 on the Card B connector should be connected to pin 5 on the Card C connector. In addition, pins 2, 4 and 5 can be left unconnected. The connections can be made by cutting pins 1, 2, 4, 5 on Card B and installing a jumper between B.X6.1 and C.X6.5. The connections will then be as follows:

- Card B X6.1 —> Card C X6.5
- Card B X6.2 —> N.C.
- Card B X6.3 —> Card C X6.3
- Card B X6.4 —> N.C.
- Card B X6.5 —> N.C.