PROOF OF CONCEPT V1

SINGLE-BOARD COMPUTER

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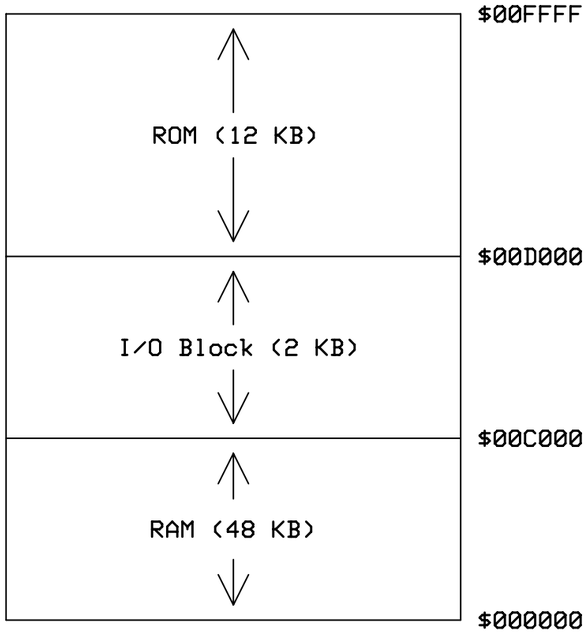
128 Kilobyte Static RAM System

Powered by the W65C816S Microprocessor

Designed by BigDumbDinosaur



ARCHITECTURE

BCS Technology Limited		
W65C816S SINGLE BOARD COMPUTER		
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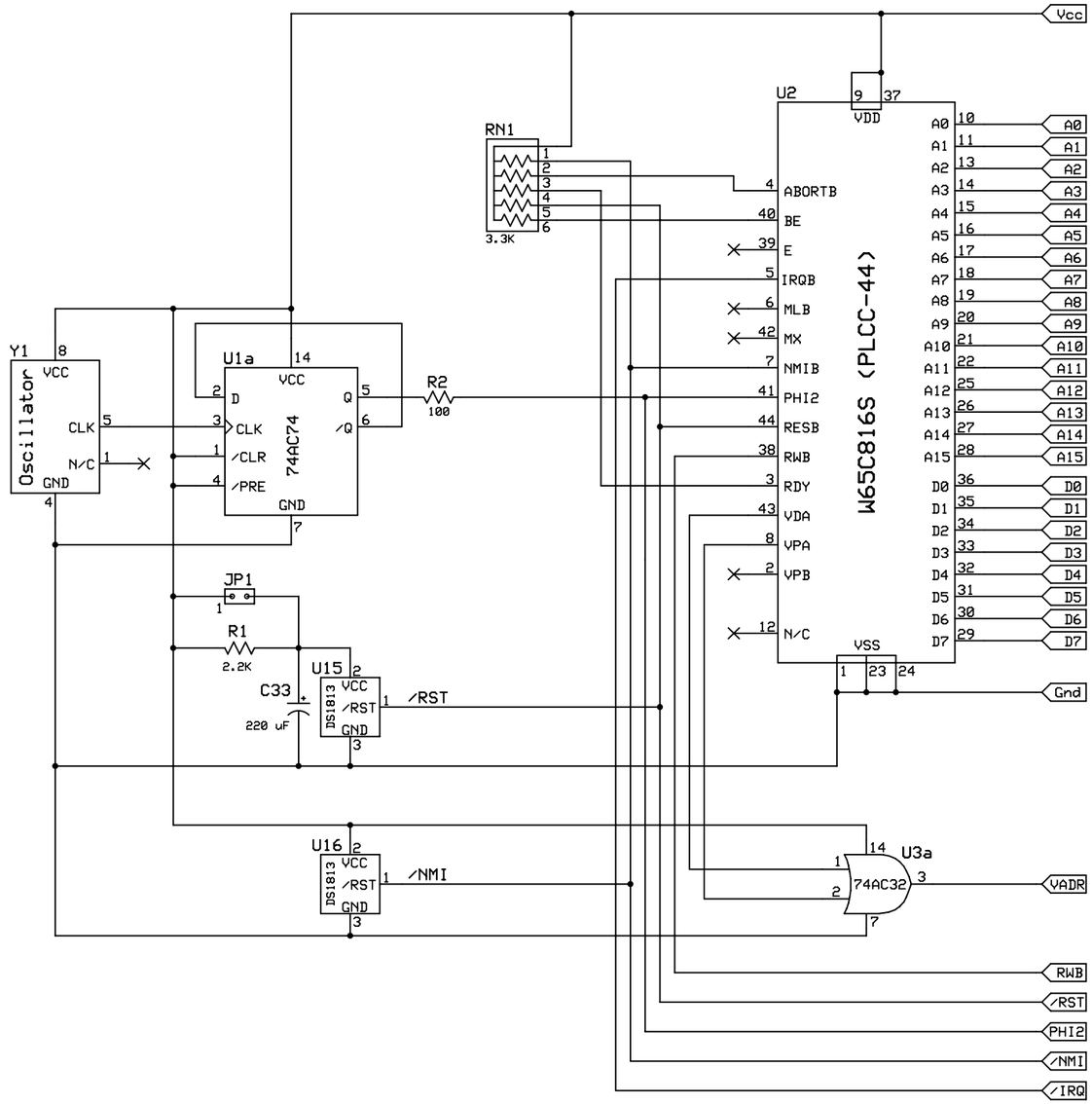
POC V1.2 MEMORY MAP

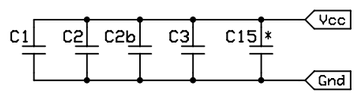
	8	4	2	1	0	0	0	0	0	0	0	0	0	0	0	0			
	0	0	0	0	8	4	2	1	0	0	0	0	0	0	0	0			
	0	0	0	0	0	0	0	0	8	4	2	1	0	0	0	0			
	0	0	0	0	0	0	0	0	0	0	0	0	8	4	2	1			SIZE
ADDRESS	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	SYMBOL	ASSIGNMENT	KB
$000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAM	RAM Start	48.00
$00BFFF	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1		RAM End	
$00C000	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IOBLK (1)	I/O Start	4.00
$00CFFF	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1		I/O End	
$00D000	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	ROM	ROM Start	12.00
$00FFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		ROM End	

1) Mirrors due to not being fully decoded.

I/O BLOCK DECODING

	8	4	2	1	0	0	0	0		
	0	0	0	0	8	4	2	1		
	0	0	0	0	0	0	0	0		
	0	0	0	0	0	0	0	0		
ADDRESS	A15	A14	A13	A12	A11	A10	A9	A8	ASSIGNMENT	SYMBOL
$00C000	1	1	0	0	0	0	0	0	vQUART Channels A-B, timer A	SIOA
$00C100	1	1	0	0	0	0	0	1	vQUART Channels C-D, timer B	SIOB
$00C200	1	1	0	0	0	0	1	0	vQUART Channel IRQ Status	SIOQ
$00C300	1	1	0	0	0	0	1	1	Real-Time Clock	RTC
$00C400	1	1	0	0	0	1	0	0	Expansion Select A	XIOA
$00C500	1	1	0	0	0	1	0	1	Expansion Select B	XIOB
$00C600	1	1	0	0	0	1	1	0	Expansion Select C	XIOC
$00C700	1	1	0	0	0	1	1	1	---	---





Decoupling Capacitors -- 0.1 uf @ 50v

*C15→Y1

MPU INTERFACE

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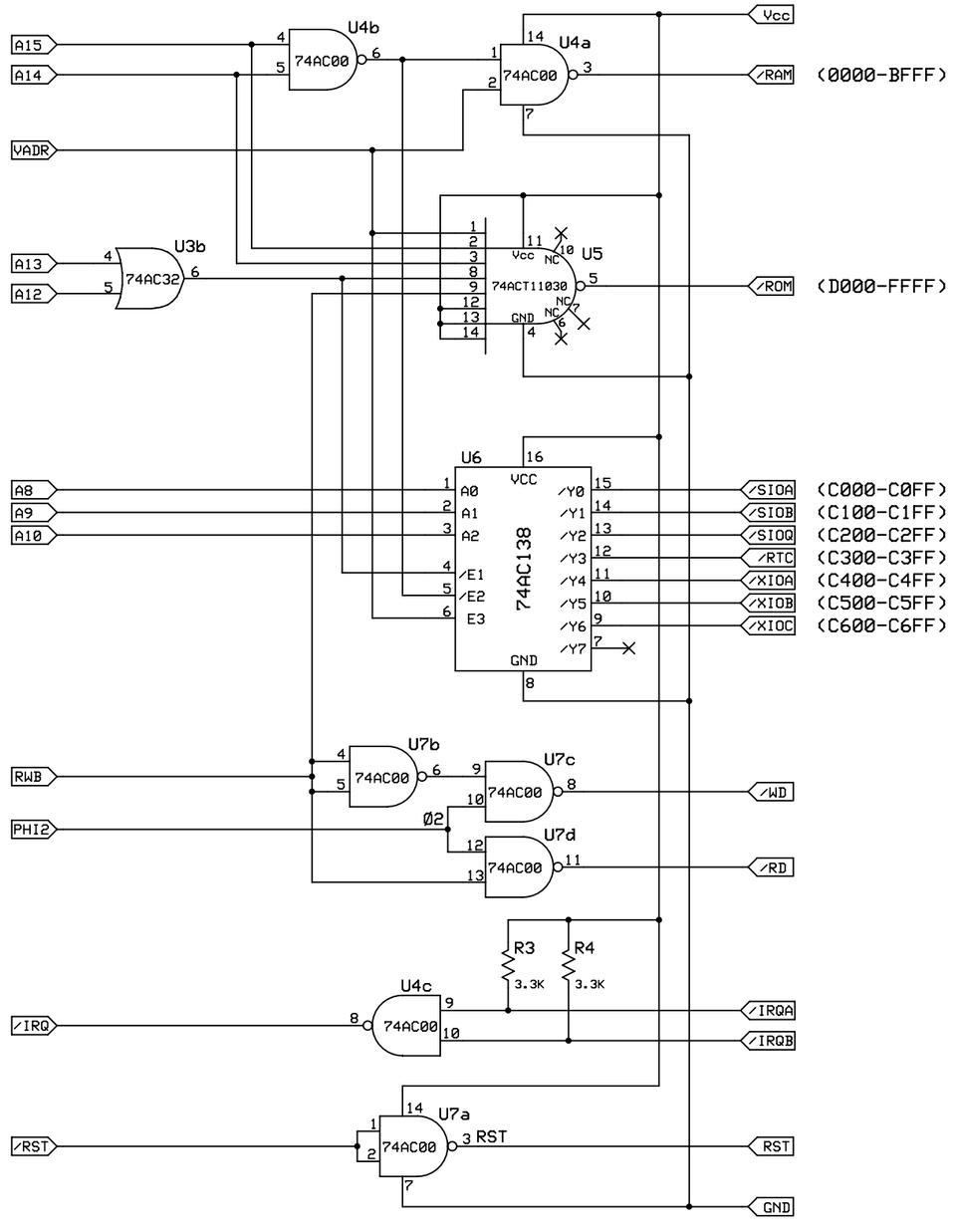

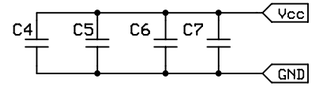

Decoupling Capacitors -- 0.1 uf @ 50v

GLUE LOGIC

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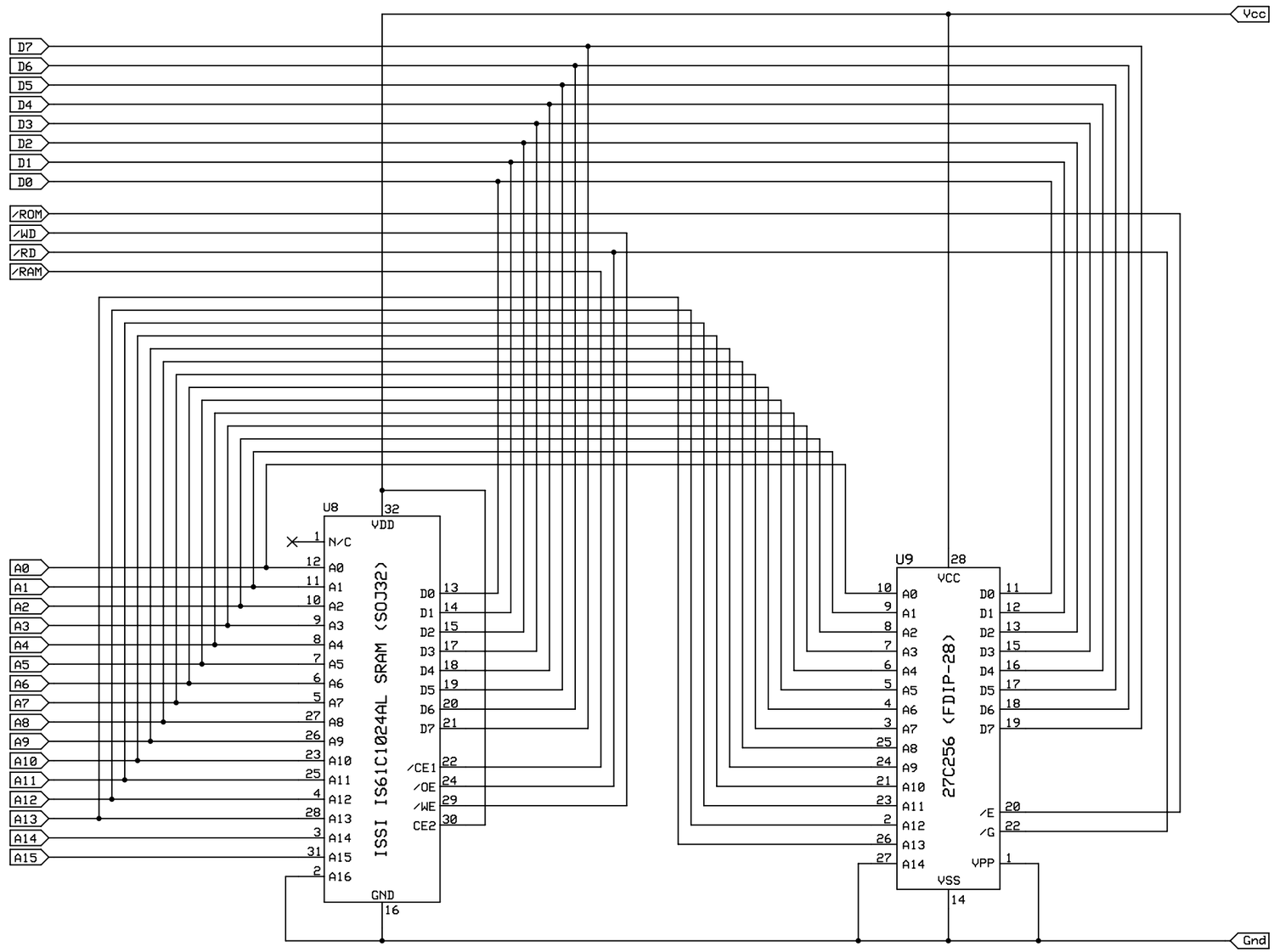

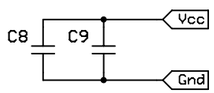

Decoupling Capacitors -- 0.1 uf @ 50v

RAM & ROM

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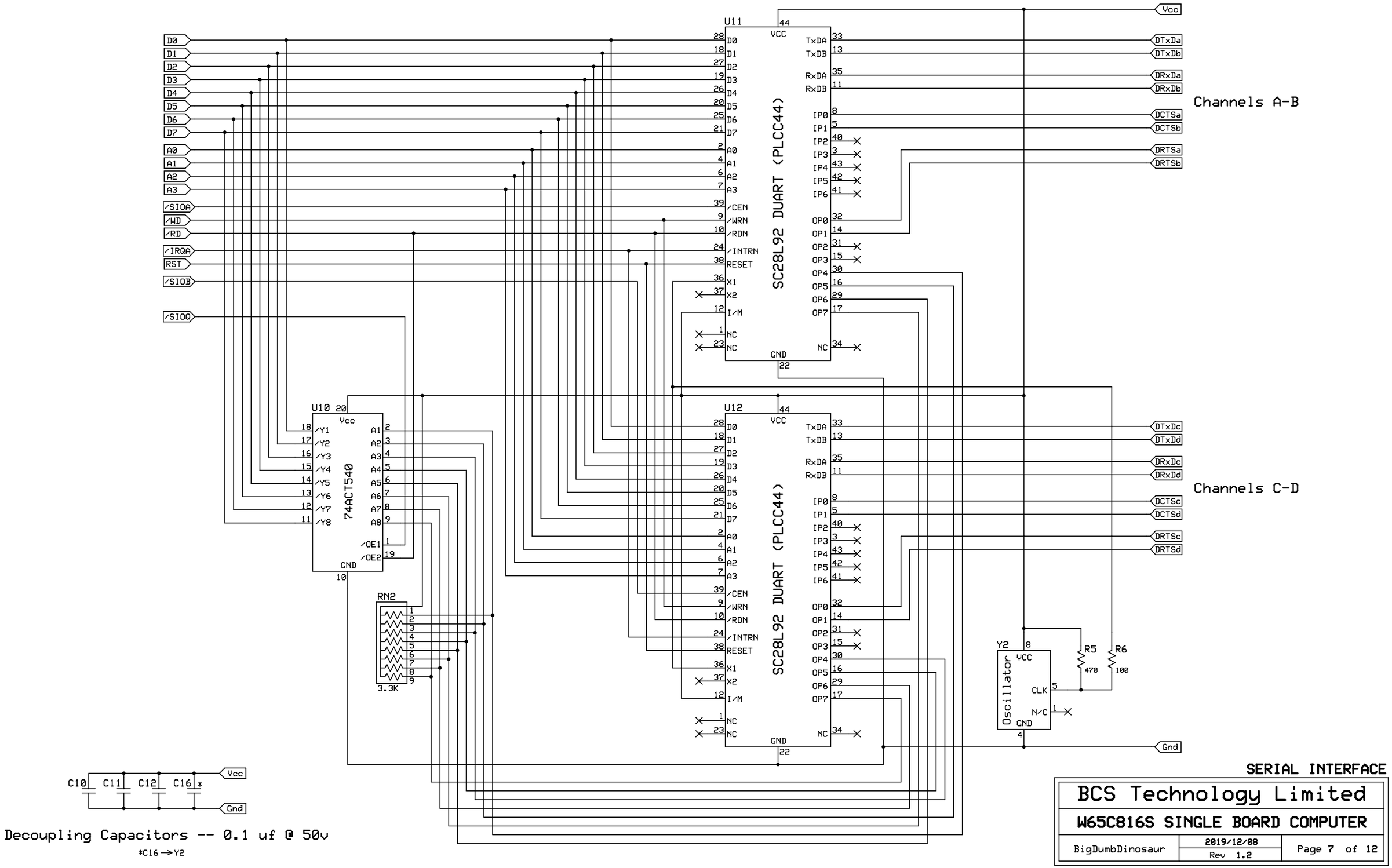
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
/SIOA
/WD
/RD
/IRQA
RST
/SIOB
/SIOQ
U11
SC28L92 DUART (PLCC44)
VCC
GND
TxDA
TxDB
RxDA
RxDB
IP0
IP1
IP2
IP3
IP4
IP5
IP6
OP0
OP1
OP2
OP3
OP4
OP5
OP6
OP7
/CEN
/WRN
/RDN
/INTRN
RESET
X1
X2
I/M
NC
Vcc
DTxDa
DTxDb
DRxDa
DRxDb
DCTSa
DCTSb
DRTSa
DRTSb
Channels A-B
U10
74ACT540
/Y1
/Y2
/Y3
/Y4
/Y5
/Y6
/Y7
/Y8
/OE1
/OE2
RN2
3.3K
U12
DTxDc
DTxDd
DRxDc
DRxDd
DCTSc
DCTSd
DRTSc
DRTSd
Channels C-D
Y2
Oscillator
CLK
N/C
R5
470
R6
100
Gnd
C10
C11
C12
C16
*
Decoupling Capacitors -- 0.1 uf @ 50v
*C16 -> Y2
SERIAL INTERFACE
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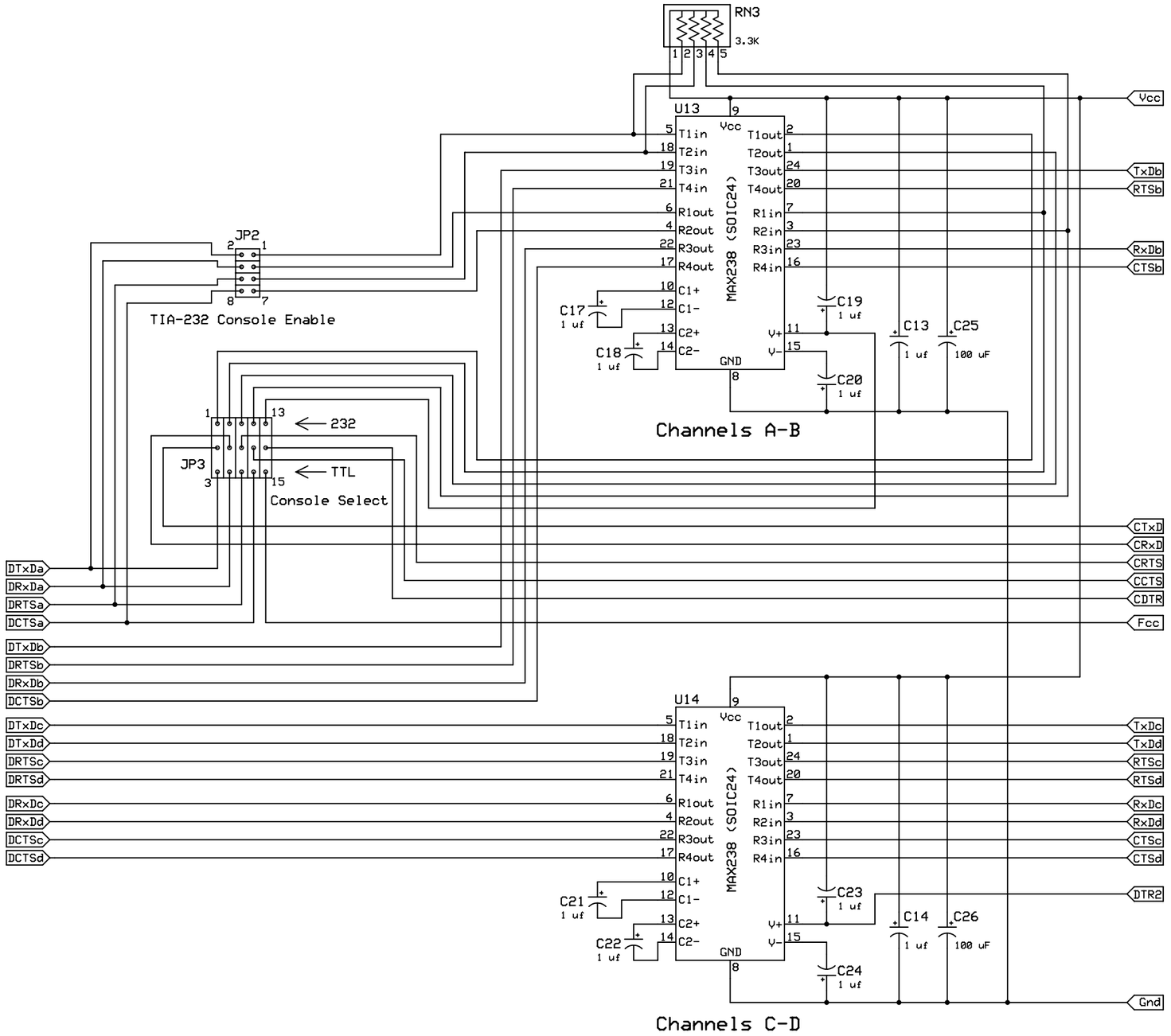

TIA232 INPUT/OUTPUT

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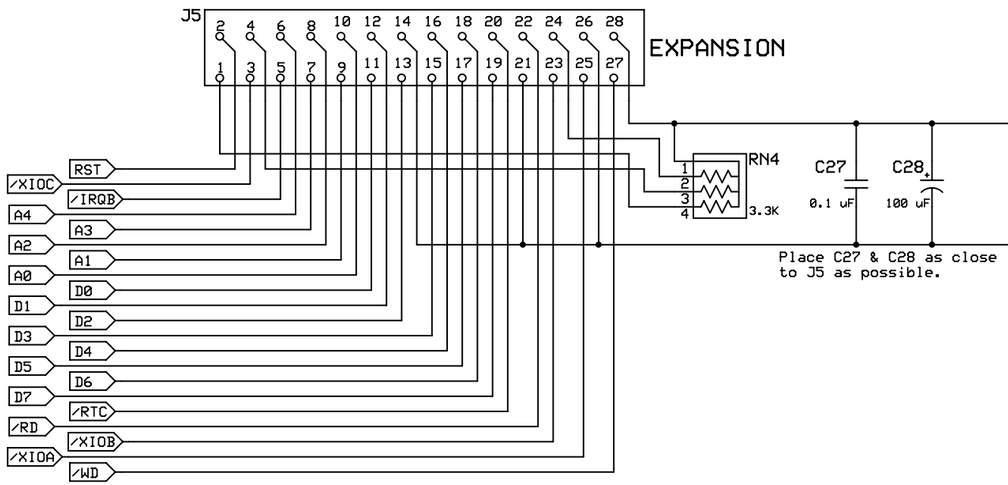

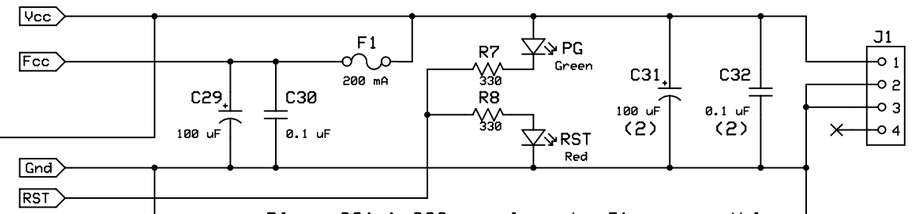

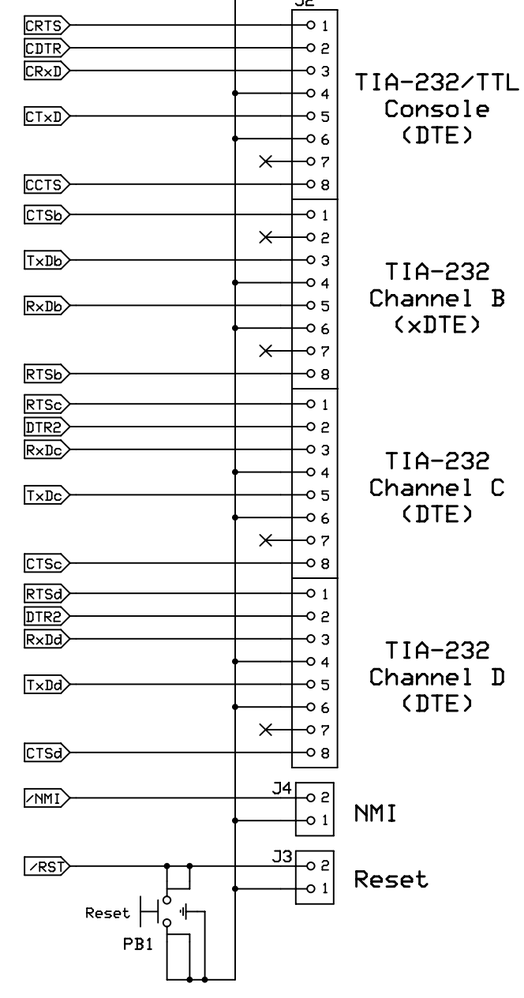

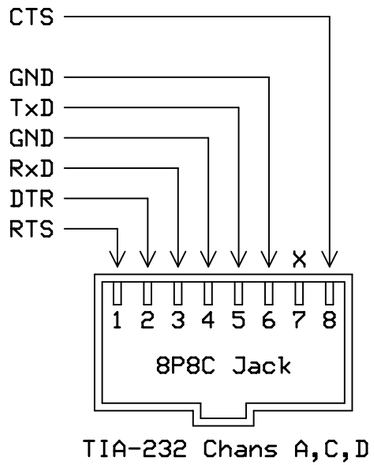

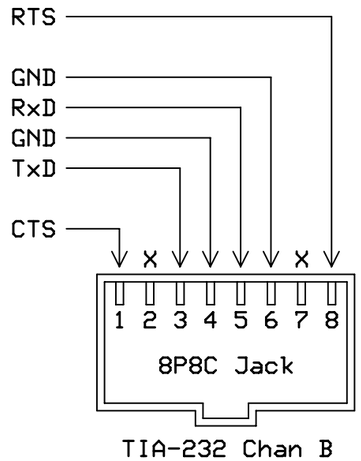

EXTERNAL INTERFACE

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