

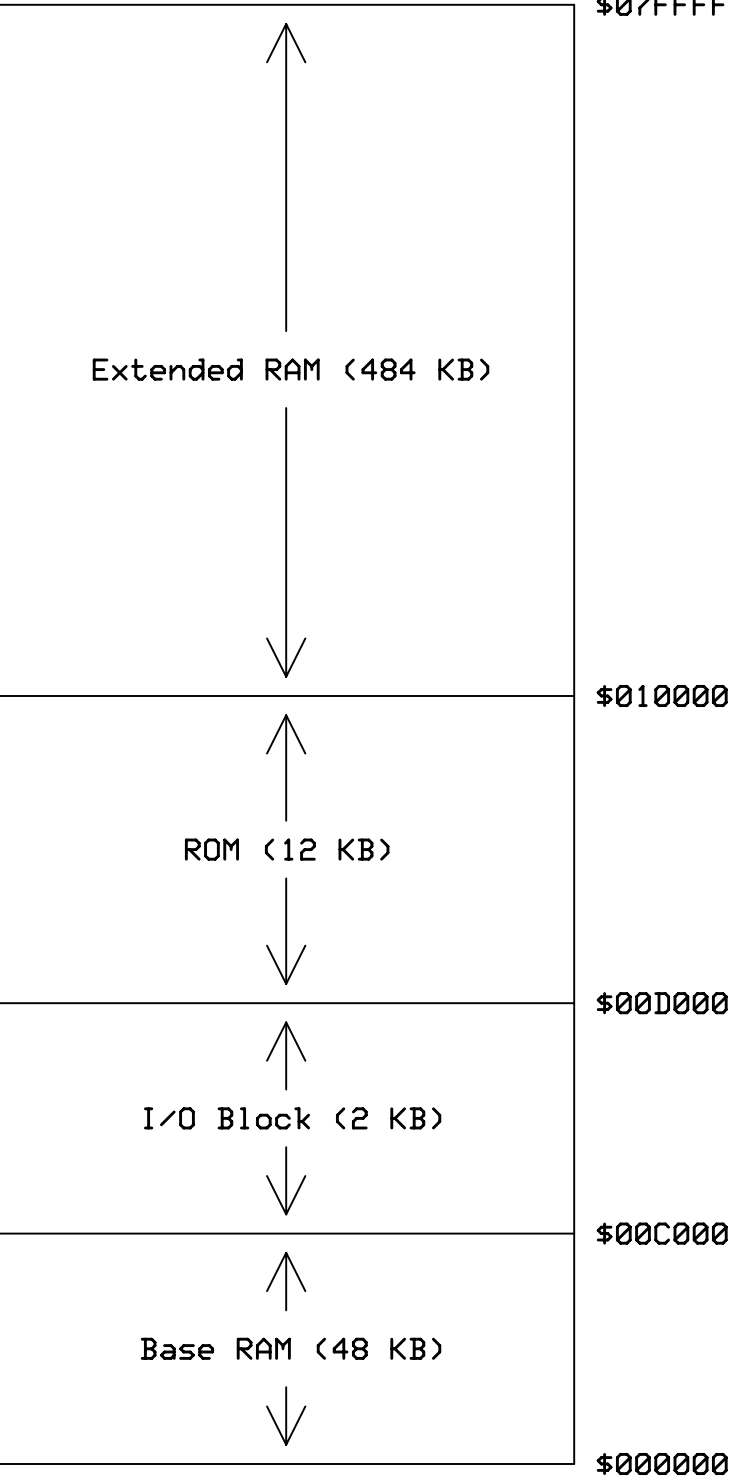
PROOF OF CONCEPT V1

SINGLE-BOARD COMPUTER

512 Kilobyte Static RAM System

Powered by the W65C816S Microprocessor

Designed by BigDumbDinosaur



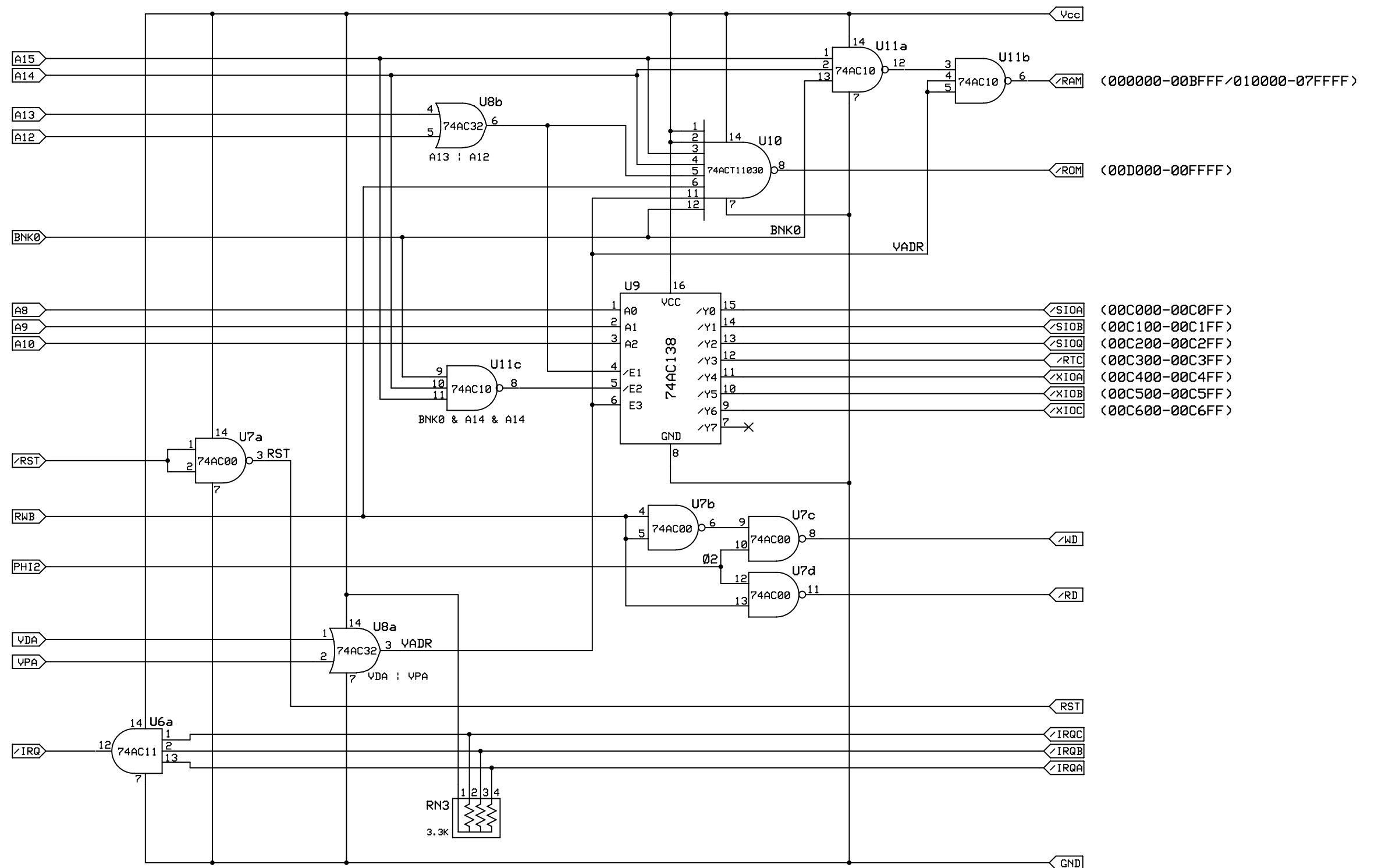
ARCHITECTURE

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W65C816S SINGLE BOARD COMPUTER		
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												POC V1 MEMORY MAP																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																								
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1) Mirrors due to not being fully decoded.

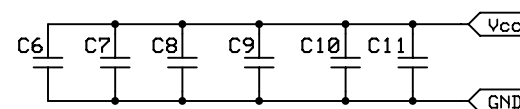
I/O BLOCK DECODING										
	8	4	2	1	0	0	0	0		
	0	0	0	0	8	4	2	1		
	0	0	0	0	0	0	0	0		
	0	0	0	0	0	0	0	0		
ADDRESS	A15	A14	A13	A12	A11	A10	A9	A8	ASSIGNMENT	SYMBOL
\$00C000	1	1	0	0	0	0	0	0	vQUART Channels A-B, timer A	SIOA
\$00C100	1	1	0	0	0	0	0	1	vQUART Channels C-D, timer B	SIOB
\$00C200	1	1	0	0	0	0	1	0	vQUART Channel IRQ Status	SIOQ
\$00C300	1	1	0	0	0	0	1	1	Real-Time Clock	RTC
\$00C400	1	1	0	0	0	1	0	0	Expansion Select A	XIOA
\$00C500	1	1	0	0	0	1	0	1	Expansion Select B	XIOB
\$00C600	1	1	0	0	0	1	1	0	Expansion Select C	XIOC
\$00C700	1	1	0	0	0	1	1	1	---	---



GLUE LOGIC EQUATIONS

$BNK0 = \neg(A18 \mid A17 \mid A16)$
 $VADR = VDA \mid VPA$
 $!RAM = VADR \& !BNK0 \mid \neg(A15 \& A14)$
 $!ROM = VADR \& BNK0 \& RWB \& A15 \& A14 \& (A13 \mid A12)$
 $IO = VADR \& BNK0 \& A15 \& A14 \& \neg(A12 \mid A13)$
 $!IRQ = \neg(IRQA \& IRQB \& IRQC)$

Symbols: & = logical AND
 | = logical OR
 ! = logical NOT



Decoupling Capacitors -- 0.1 uf @ 50v

GLUE LOGIC

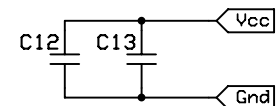
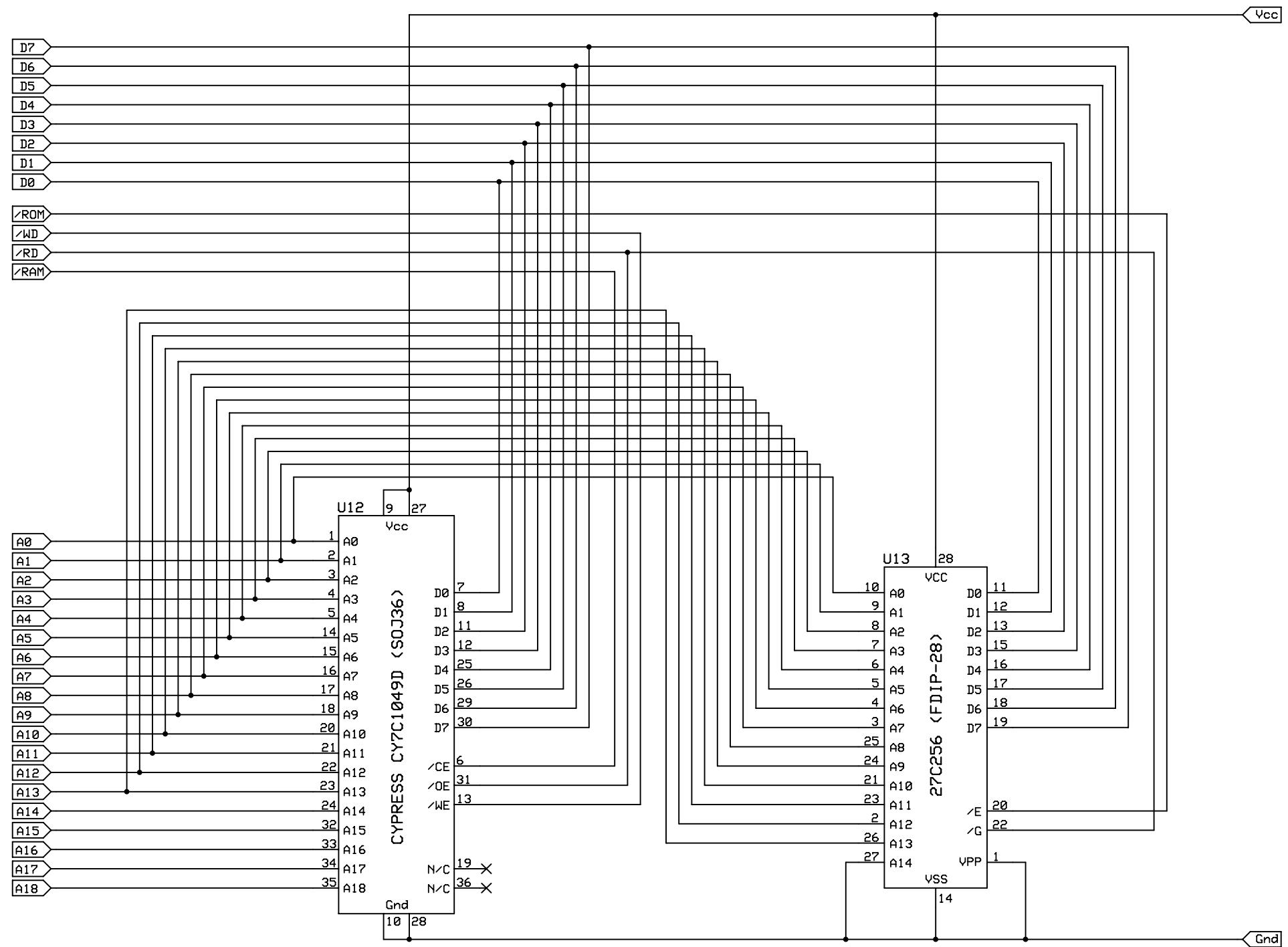
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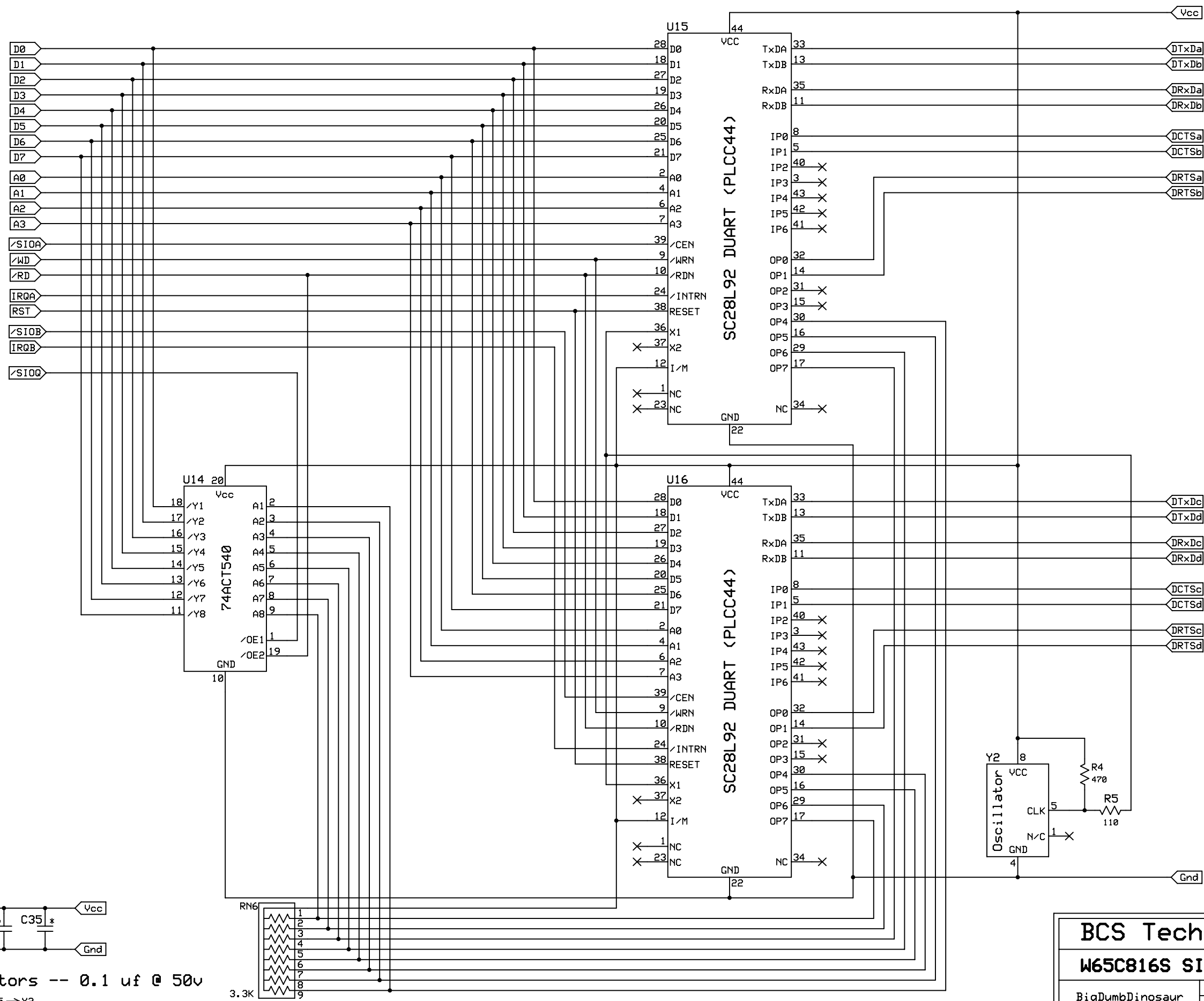
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Decoupling Capacitors -- 0.1 uf @ 50v

RAM & ROM

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Channels A-B

Channels C-D

Decoupling Capacitors -- 0.1 uf @ 50v

*C35 → Y2

SERIAL INTERFACE

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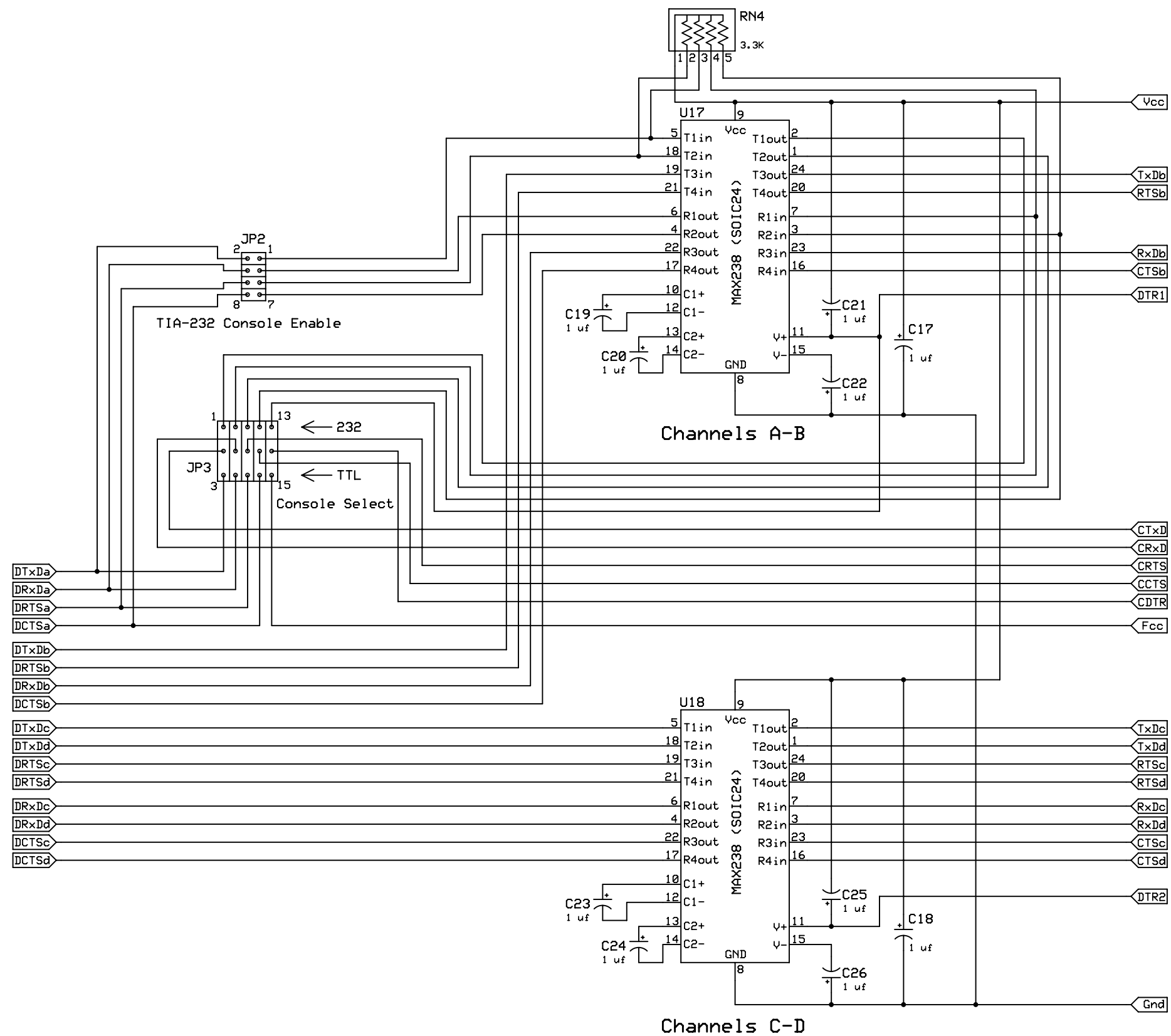
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TIA232 INPUT/OUTPUT

