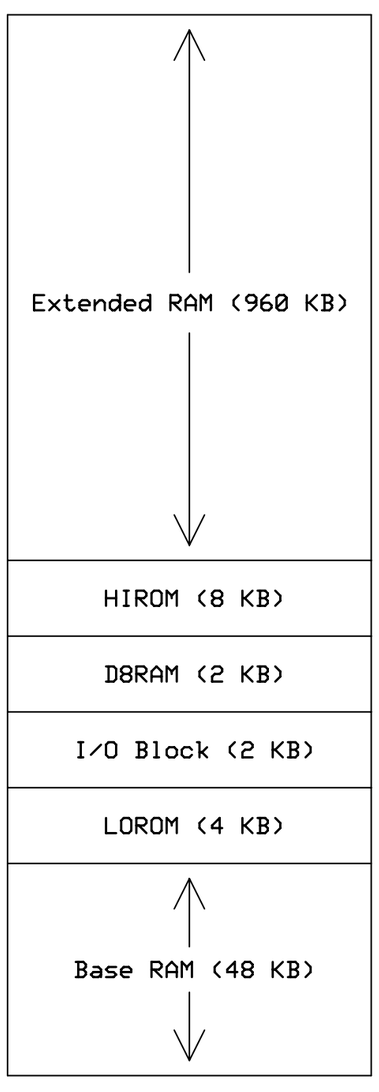
PROOF OF CONCEPT V2

SINGLE-BOARD COMPUTER

One Megabyte Static RAM System

Powered by the W65C816S Microprocessor

Designed by BigDumbDinosaur



$0FFFFF

$010000 (EXRAM)

$00E000 (HIROM)

$00D800 (D8RAM)

$00D000 (IOBLK)

$00C000 (LOROM)

$000000 (BASRAM)

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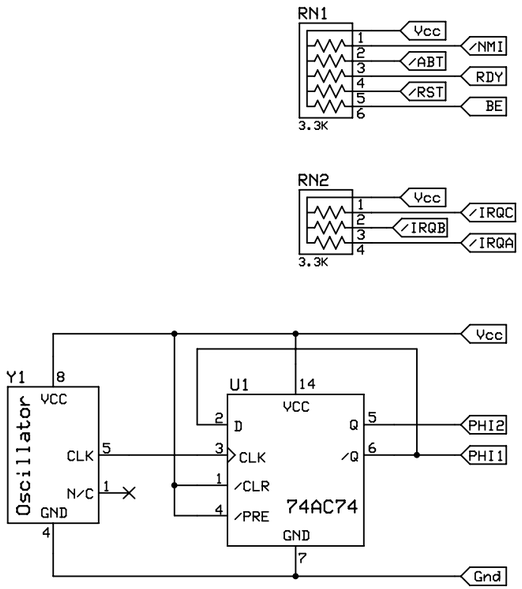
POC V2.2 MEMORY MAP

	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	8	4	2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
	0	0	0	0	8	4	2	1	0	0	0	0	0	0	0	0	0	0	0	0			
	0	0	0	0	0	0	0	0	8	4	2	1	0	0	0	0	0	0	0	0			
	0	0	0	0	0	0	0	0	0	0	0	0	8	4	2	1	0	0	0	0			
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8	4	2	1			
ADDRESS	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	SYMBOL	ASSIGNMENT	KB
$000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BASRAM	Base RAM Start	48
$00BFFF	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1		Base RAM End	
$00C000	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LOROM	Low ROM Start	4
$00CFFF	0	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1		Low ROM End	
$00D000	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	IOBLK	I/O Start	2
$00D7FF	0	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1		I/O End	
$00D800	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	D8RAM	D8RAM Start	2
$00DFFF	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1		D8RAM End	
$00E000	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	HIROM	High ROM Start	8
$00FFFF	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		High ROM End	
$010000	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EXRAM	Extended RAM Start	960
$0FFFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		Extended RAM End	

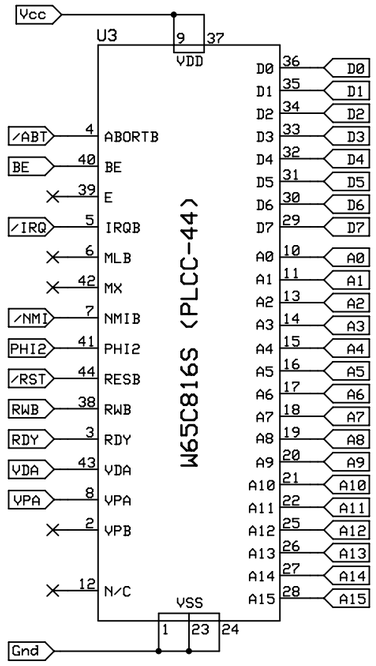
I/O BLOCK DECODING

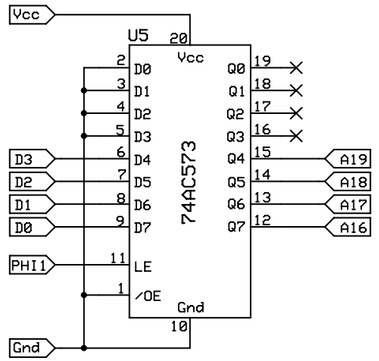
	8	4	2	1	0	0	0	0		
	0	0	0	0	8	4	2	1		
	0	0	0	0	0	0	0	0		
	0	0	0	0	0	0	0	0		
ADDRESS	A15	A14	A13	A12	A11	A10	A9	A8	ASSIGNMENT	SYMBOL
$00D000	1	1	0	1	0	0	0	0	SC28L92 DUART A-B, timer A	SIOA
$00D100	1	1	0	1	0	0	0	1	SC28L92 DUART C-D, timer B	SIOB
$00D200	1	1	0	1	0	0	1	0	DS1511Y RTC	RTC
$00D300	1	1	0	1	0	0	1	1	Expansion A	XIOA
$00D400	1	1	0	1	0	1	0	0	Expansion B	XIOB
$00D500	1	1	0	1	0	1	0	1	Expansion C	XIOC
$00D600	1	1	0	1	0	1	1	0	---	---
$00D700	1	1	0	1	0	1	1	1	---	---



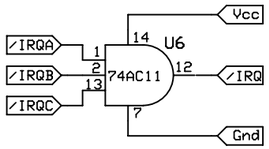
Ø2 Clock Generator

CLK = PHI2 =

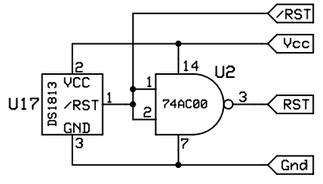




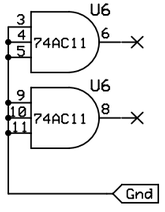
Extended Address Generation

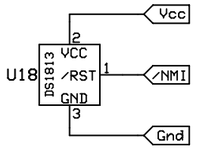


IRQ Driver

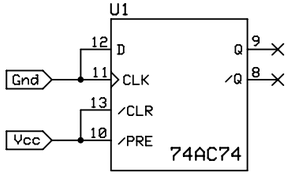


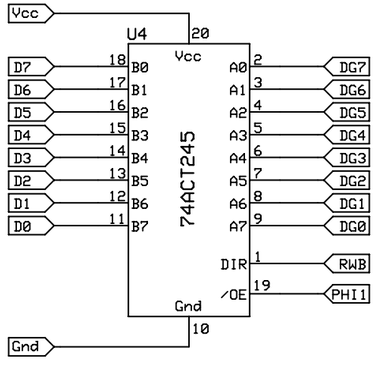
Reset Generator



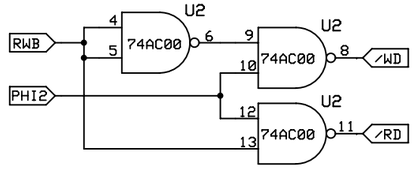


NMI Debouncer



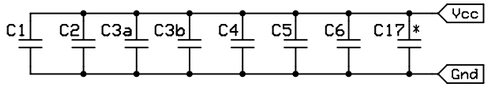


Data Bus Driver



RWB	PHI2	/RD	/WD
X	L	H	H
H	H	L	H
L	H	H	L

Read/Write Logic



Decoupling Capacitors -- 0.1 uf @ 50v

*C17 → Y1

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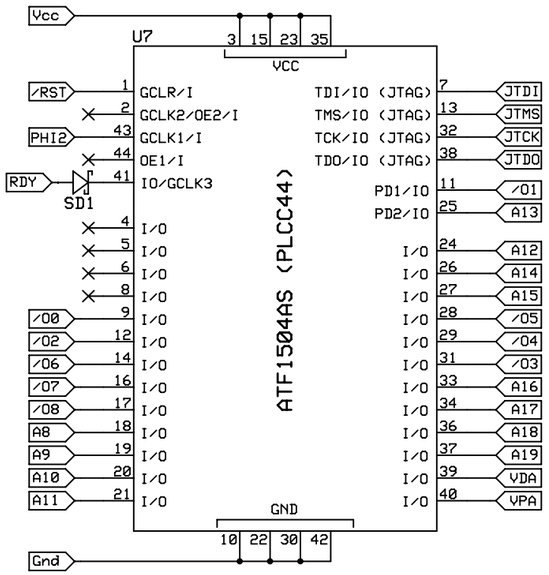

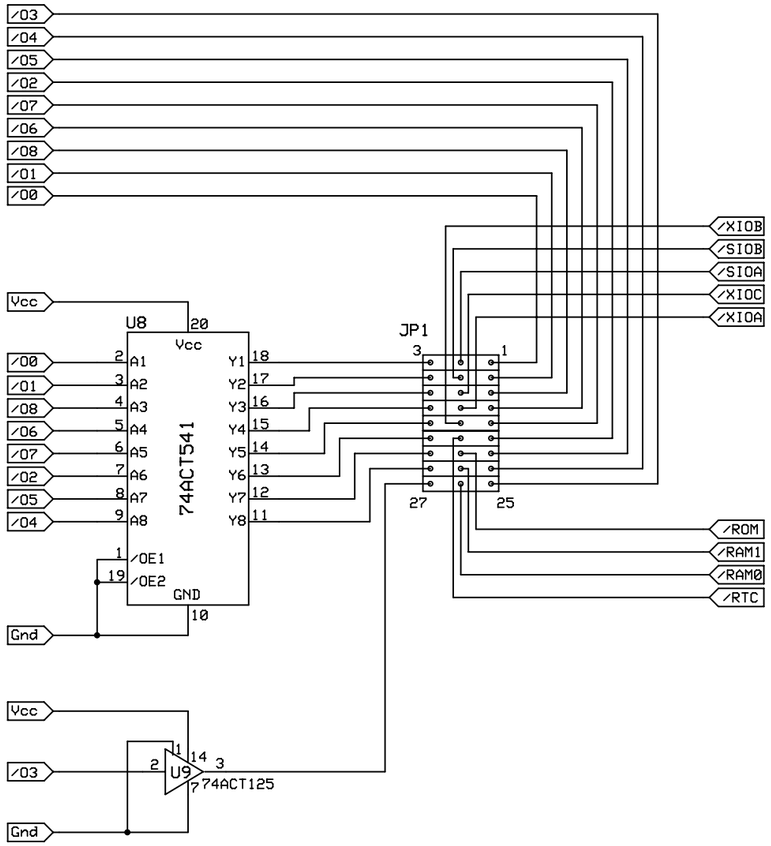

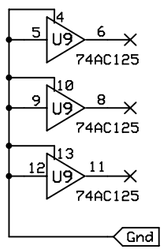

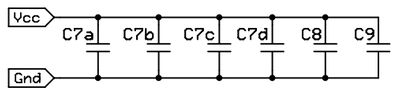

Decoupling Capacitors -- 0.1 uf @ 50v

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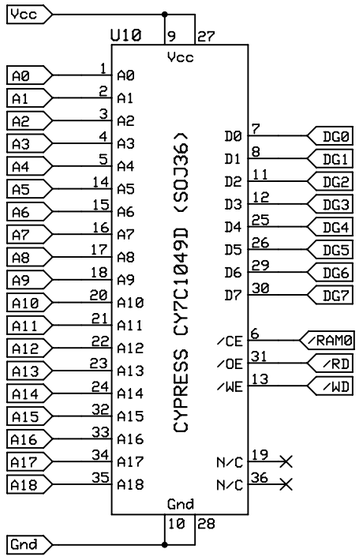
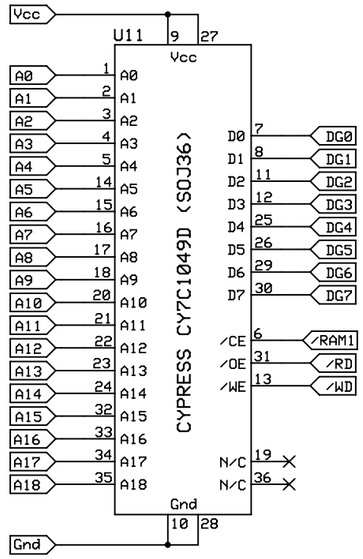
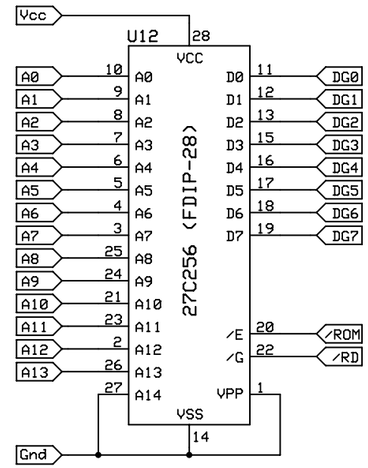


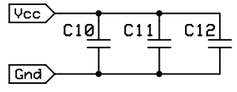
BASRAM ($000000-$00BFFF)
D8RAM ($00D800-$00DFFF)
EXRAM ($010000-$07FFFF)



EXRAM ($080000-$0FFFFF)



LOROM ($00C000-$00CFFF)
HIROM ($00E000-$00FFFF)



Decoupling Capacitors -- 0.1 uf @ 50v

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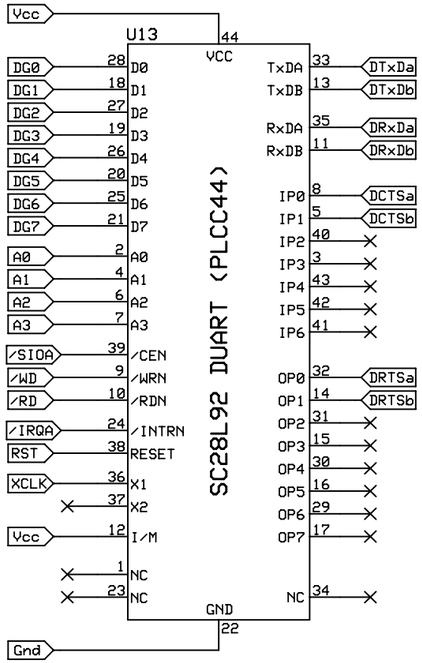
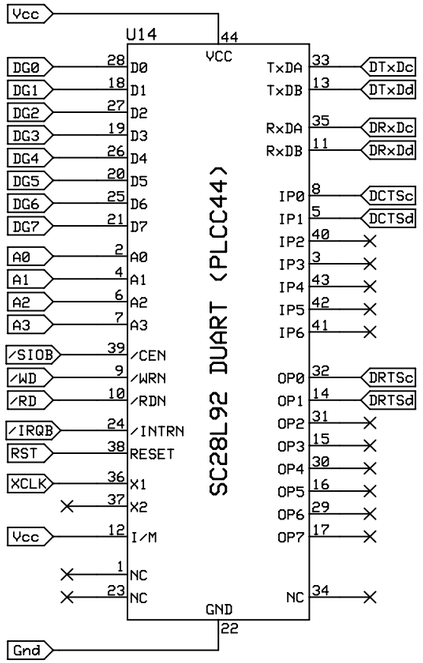
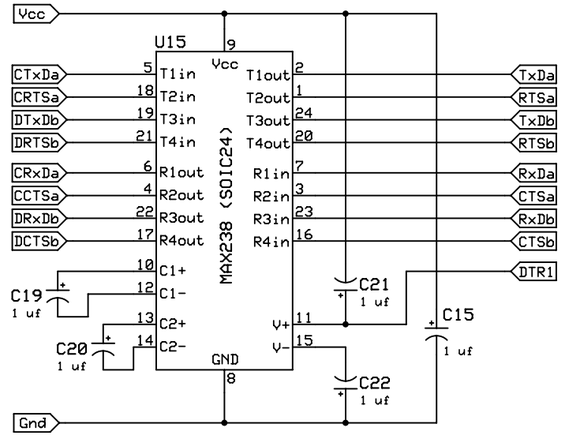


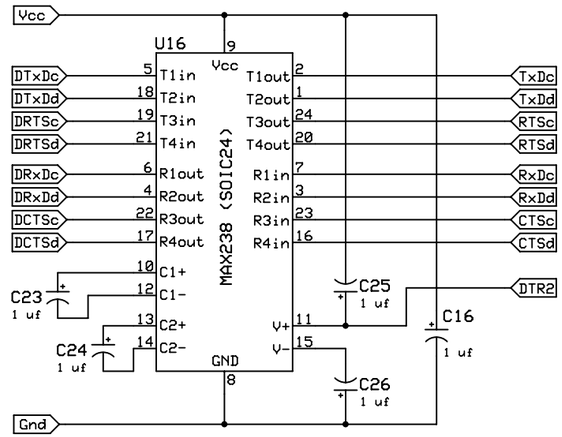
Channels A-B ($00D000)



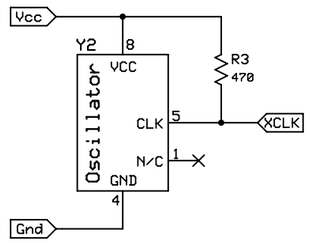
Channels C-D ($00D100)

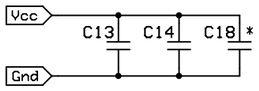


Channels A-B



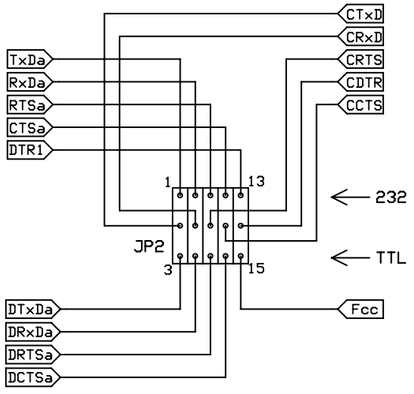
Channels C-D



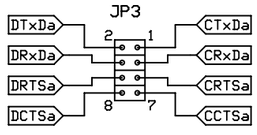


Decoupling Capacitors -- 0.1 uf @ 50v

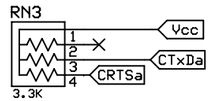
*C18 -> Y2



Console Select



TIA-232 Console Enable



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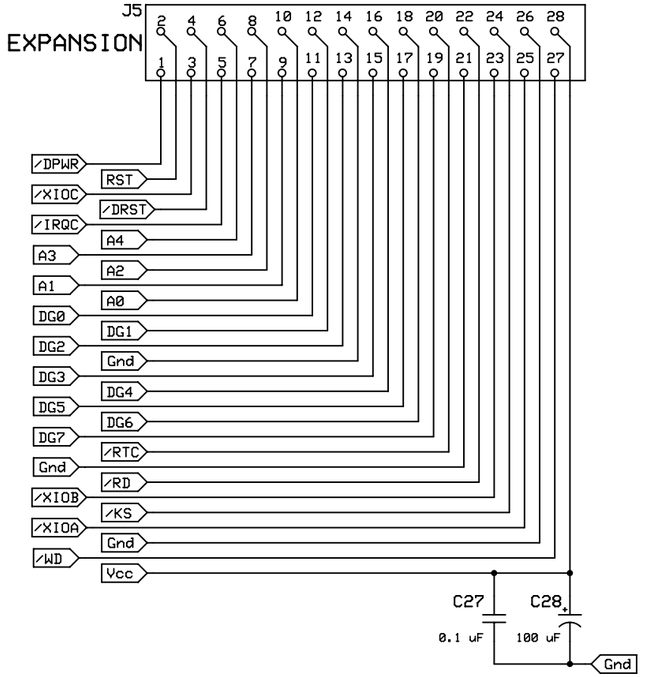
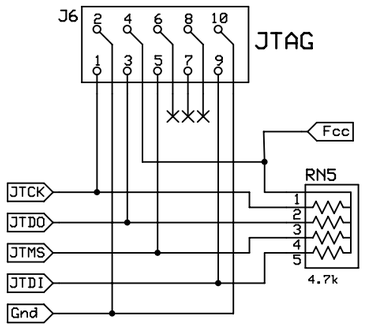
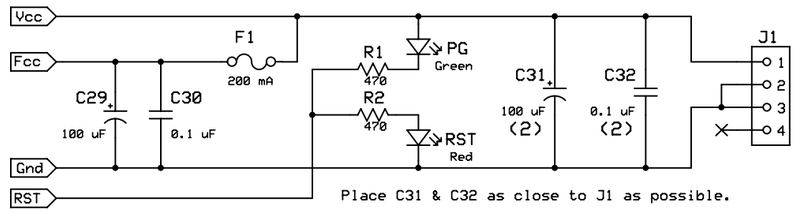
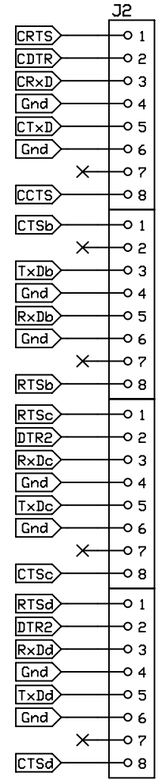






5.0 VDC
Power In

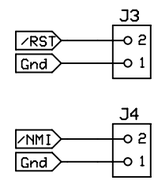


TIA-232/TTL
Console
(DTE)

TIA-232
Channel B
(xDTE)

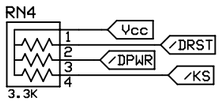
TIA-232
Channel C
(DTE)

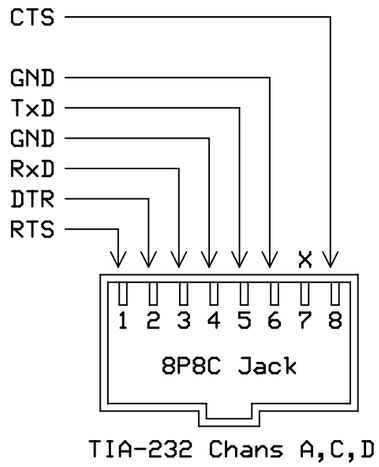
TIA-232
Channel D
(DTE)



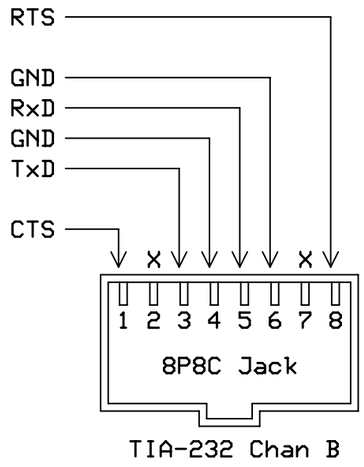
Reset

NMI





TIA-232 Chans A,C,D



TIA-232 Chan B

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