

HM4864-2, HM4864-3 HM4864P-2, HM4864P-3

65536-word × 1-bit Dynamic Random Access Memory

The HM4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.

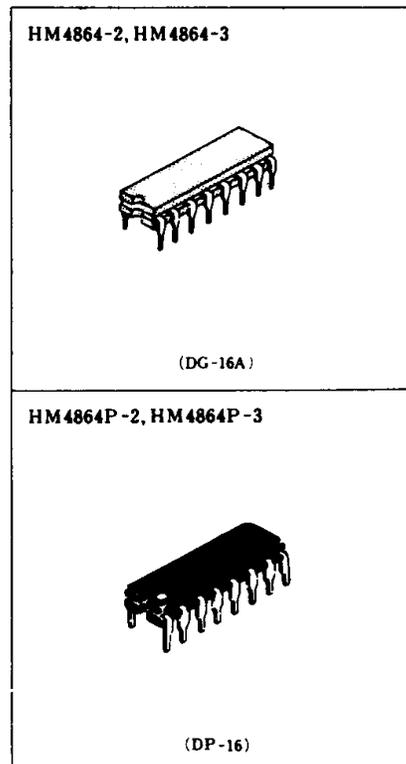
This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of +5V with $\pm 10\%$ tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.

In addition to the usual read, write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and RAS-only refresh.

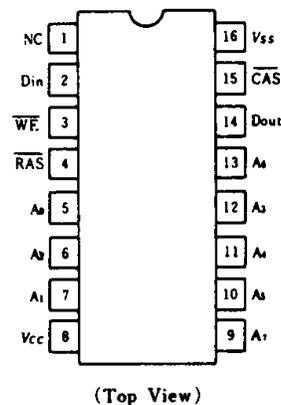
Proper control of the clock inputs ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

■ FEATURES

- Recognized industry standard 16-pin configuration
- 150ns access time, 270ns cycle time (HM4864-2, HM4864P-2)
- 200ns access time, 335ns cycle time (HM4864-3, HM4864P-3)
- Single power supply of +5V $\pm 10\%$ with a built-in V_{BB} generator
- Low Power; 330 mW active. 20 mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge
- Output data controlled by $\overline{\text{CAS}}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{\text{RAS}}$ -only refresh, and Page-mode capability
- 128 refresh cycle

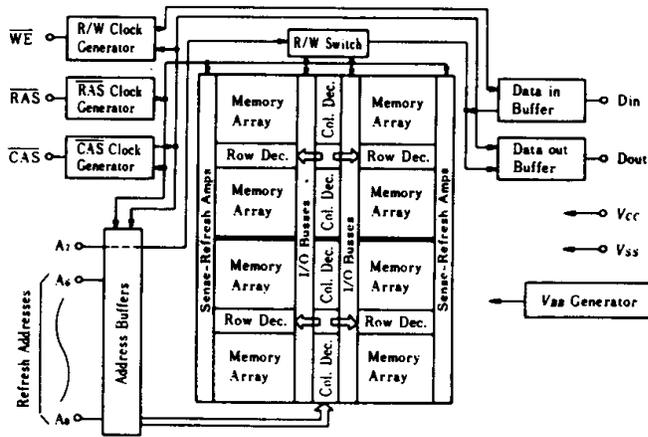


■ PIN ARRANGEMENT



A ₀ -A ₇	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{WE}}$	Read/Write Input
V _{CC}	Power (+5V)
V _{SS}	Ground
A ₀ -A ₁	Refresh Address Input

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

- Voltage on any pin relative to V_{SS} -1.0 to +7V
- Operating Temperature, T_a (Ambient) 0 to +70°C
- Storage Temperature (Ambient) -65 to +150°C (Cerdip)
-55 to +125°C (Plastic)
- Short-circuit Output Current 50 mA
- Power Dissipation 1 W

RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to +70°C)

Parameter	Symbol	min	typ	max	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

DC ELECTRICAL CHARACTERISTICS ($T_a=0$ to +70°C, $V_{CC}=5V \pm 10\%$, $V_{SS}=0V$)

Parameter	Symbol	min	max	Unit	Notes
OPERATING CURRENT					
Average Power Supply Operating Current ($\overline{RAS}, \overline{CAS}$ Cycling; $t_{RC} = \text{min.}$)	I_{CC1}	—	60	mA	2, 4
STANDBY CURRENT					
Power Supply Standby Current ($\overline{RAS} = V_{IH}$, $D_{out} = \text{High Impedance}$)	I_{CC2}	—	3.5	mA	2
REFRESH CURRENT					
Average Power Supply Current, Refresh Mode (\overline{RAS} Cycling, $CAS = V_{IH}$; $t_{RC} = \text{min.}$)	I_{CC3}	—	45	mA	2, 4
PAGE MODE CURRENT					
Average Power Supply Current, Page-mode Operation ($\overline{RAS} = V_{IL}$, \overline{CAS} Cycling; $t_{PC} = \text{min.}$)	I_{CC4}	—	45	mA	2, 4
INPUT LEAKAGE					
Input Leakage Current, any Input ($V_{i,} = 0$ to +6.5V, all other pins not under test = 0V)	I_{LI}	-10	10	μA	
OUTPUT LEAKAGE					
Output Leakage Current (D_{out} is disabled, $V_{out} = 0$ to +5.5V)	I_{LO}	-10	10	μA	3
OUTPUT LEVELS					
Output High (Logic 1) Voltage ($I_{out} = -5\text{mA}$)	V_{OH}	2.4	V_{CC}	V	
Output Low (Logic 0) Voltage ($I_{out} = 4.2\text{mA}$)	V_{OL}	0	0.4	V	

NOTES

1. All voltages referenced to V_{SS} .
2. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
3. I_{LO} consists of leakage current only.
4. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	typ	max	Unit	Notes
Input Capacitance ($A_0 - A_7, D_{in}$)	$C_{i,1}$	—	7	pF	1
Input Capacitance ($\overline{RAS}, \overline{CAS}, \overline{WE}$)	$C_{i,2}$	—	10	pF	1
Output Capacitance (D_{out})	C_{out}	—	7	pF	1, 2

NOTES

1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable D_{OUT} .

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS ^{1), 2)}(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

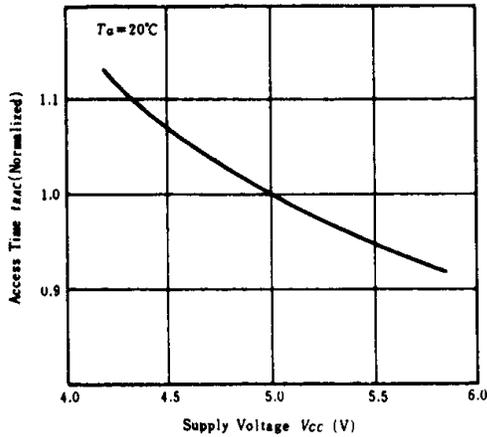
Parameter	Symbol	HM4864-2/P-2		HM4864-3/P-3		Unit	Notes
		min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	270	—	335	—	ns	
Read-Write Cycle Time	t_{RWC}	270	—	335	—	ns	
Page Mode Cycle Time	t_{PC}	170	—	225	—	ns	
Access Time from \overline{RAS}	t_{RAC}	—	150	—	200	ns	4, 6
Access Time from \overline{CAS}	t_{CAC}	—	100	—	135	ns	5, 6
Output Buffer Turn-off Delay	t_{OFF}	0	40	0	50	ns	7
Transition Time (Rise and Fall)	t_T	3	35	3	50	ns	3
\overline{RAS} Precharge Time	t_{RP}	100	—	120	—	ns	
\overline{RAS} Pulse Width	t_{RAS}	150	10000	200	10000	ns	
\overline{RAS} Hold Time	t_{RSH}	100	—	135	—	ns	
\overline{CAS} Pulse Width	t_{CAS}	100	—	135	—	ns	
\overline{CAS} Hold Time	t_{CSH}	150	—	200	—	ns	
\overline{RAS} to \overline{CAS} Delay Time	t_{RCD}	20	50	25	65	ns	8
\overline{CAS} to \overline{RAS} Precharge Time	t_{CRP}	-20	—	-20	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	20	—	25	—	ns	
Column Address Set-up Time	t_{ASC}	-10	—	-10	—	ns	
Column Address Hold Time	t_{CAH}	45	—	55	—	ns	
Column Address Hold Time referenced to \overline{RAS}	t_{AR}	95	—	120	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	45	—	55	—	ns	
Write Command Hold Time referenced to \overline{RAS}	t_{WR}	95	—	120	—	ns	
Write Command Pulse Width	t_{WP}	45	—	55	—	ns	
Write Command to \overline{RAS} Lead Time	t_{RWL}	45	—	55	—	ns	
Write Command to \overline{CAS} Lead Time	t_{CWL}	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	45	—	55	—	ns	9
Data-in Hold Time referenced to \overline{RAS}	t_{DHR}	95	—	120	—	ns	
\overline{CAS} Precharge Time (for Page-mode Cycle Only)	t_{CP}	60	—	80	—	ns	
Refresh Period	t_{REF}	—	2	—	2	ms	
Write Command Set-up Time	t_{WCS}	-20	—	-20	—	ns	10
\overline{CAS} to \overline{WE} Delay	t_{CWD}	60	—	80	—	ns	10
\overline{RAS} to \overline{WE} Delay	t_{RWD}	110	—	145	—	ns	10
\overline{RAS} Precharge to \overline{CAS} Hold Time	t_{RPC}	0	—	0	—	ns	

NOTES

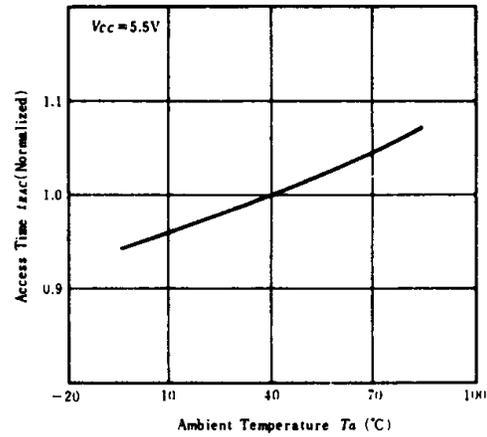
- AC measurements assume $t_T = 5ns$.
- 8 cycles are required after power-on or prolonged periods (greater than 2ms) of \overline{RAS} inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
- V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Assumes that $t_{RCD} \leq t_{RCD}(\max)$. If t_{RCD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.
- Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
- Measured with a load circuit equivalent to 2TTL loads and 100 pF.
- $t_{OFF}(\max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- Operation with the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
- These parameters are reference to \overline{CAS} leading edge in early write cycles and to \overline{WE} leading edge in delayed write or read-modify-write cycles.
- t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\min)$ and $t_{RWD} \geq t_{RWD}(\min)$ the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

■ TYPICAL CHARACTERISTICS

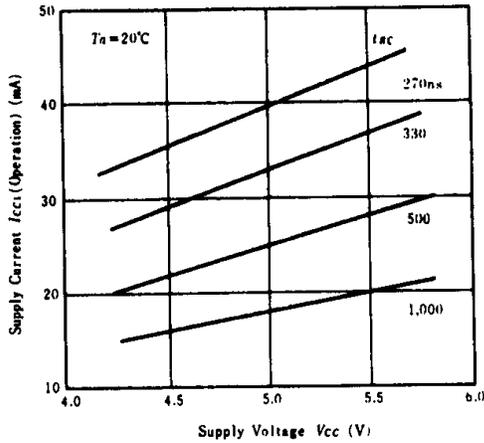
ACCESS TIME
vs. SUPPLY VOLTAGE



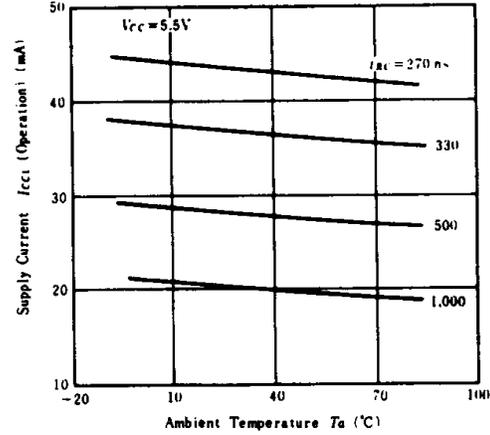
ACCESS TIME
vs. AMBIENT TEMPERATURE



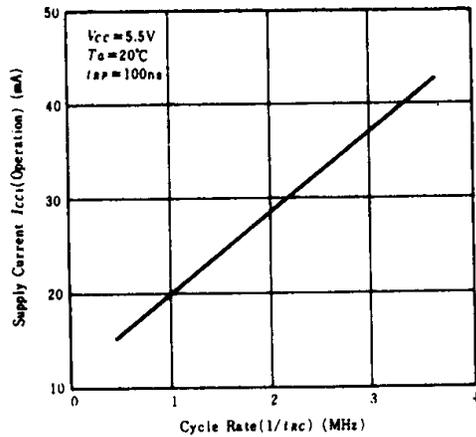
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



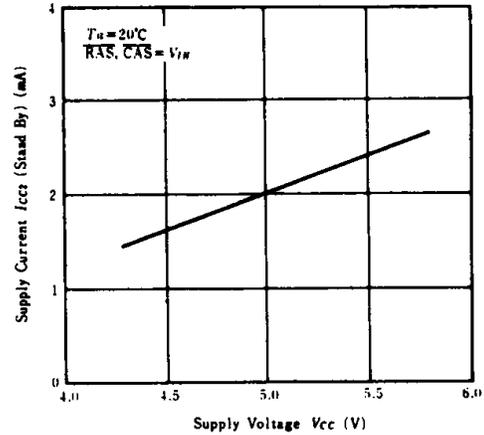
SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



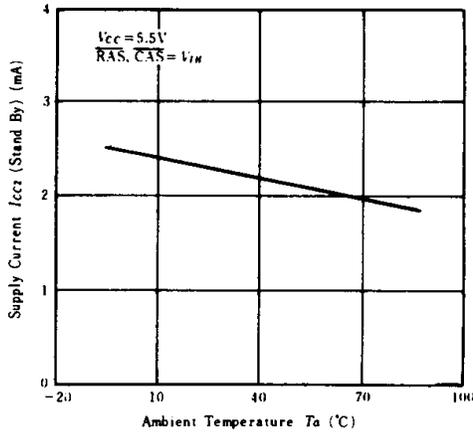
SUPPLY CURRENT
vs. CYCLE RATE



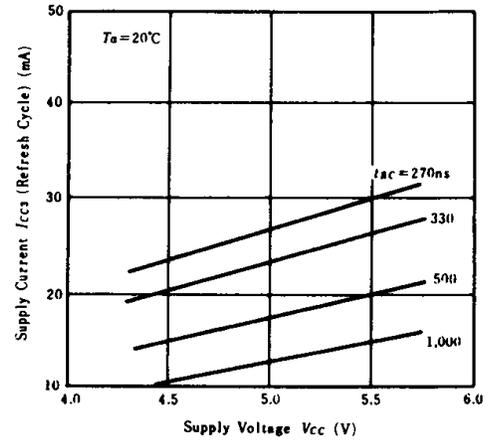
SUPPLY CURRENT
vs. SUPPLY VOLTAGE



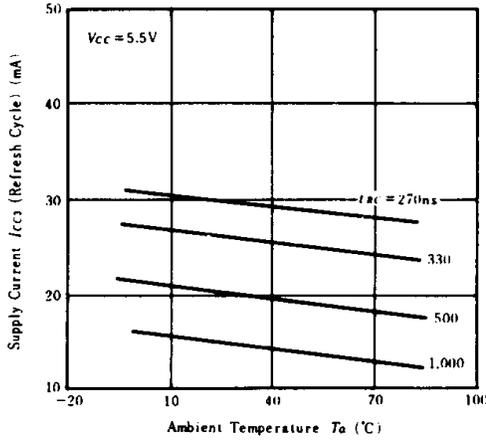
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



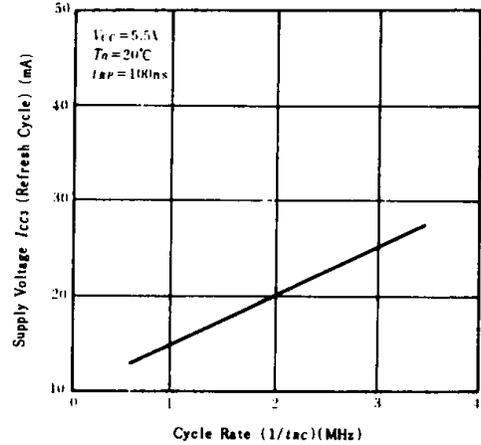
SUPPLY CURRENT vs. SUPPLY VOLTAGE



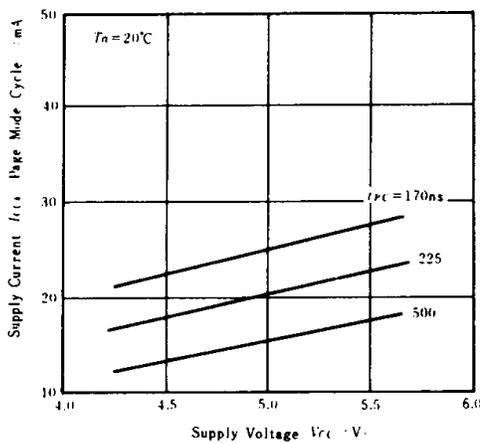
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



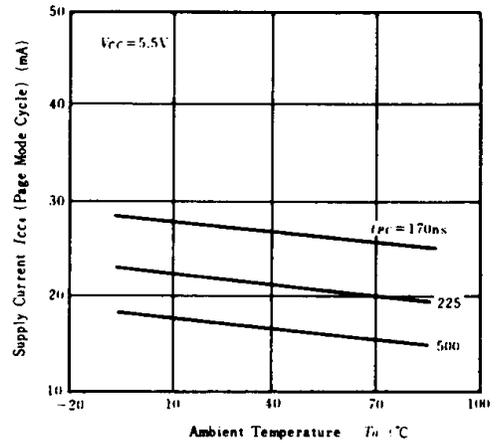
SUPPLY CURRENT vs. CYCLE RATE



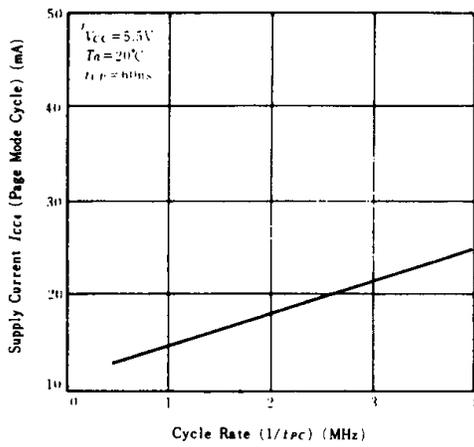
SUPPLY CURRENT vs. SUPPLY VOLTAGE



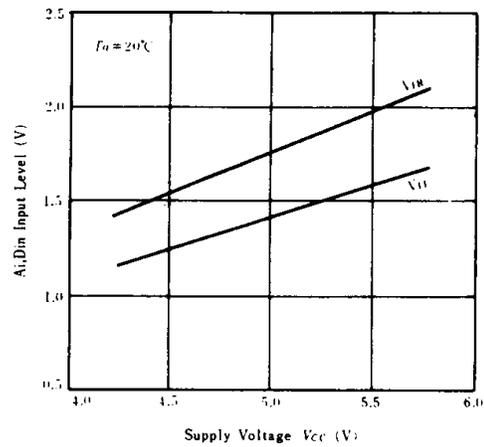
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



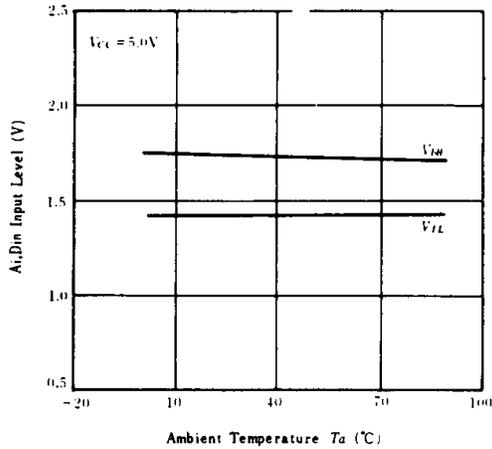
SUPPLY CURRENT vs. CYCLE RATE



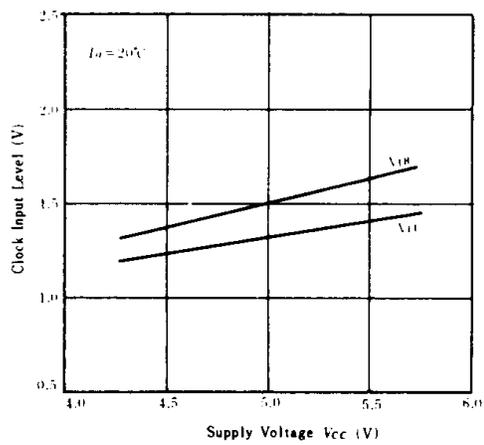
INPUT LEVEL vs. SUPPLY VOLTAGE



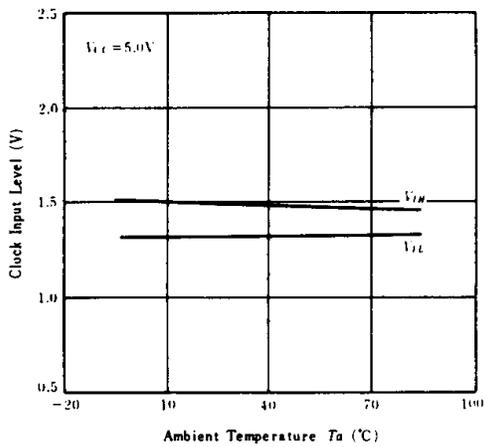
INPUT LEVEL vs. AMBIENT TEMPERATURE

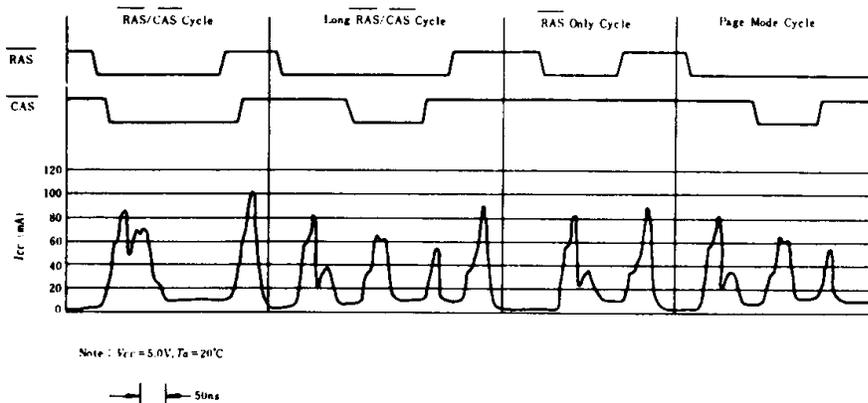


CLOCK INPUT LEVEL vs. SUPPLY VOLTAGE



CLOCK INPUT LEVEL vs. AMBIENT TEMPERATURE





■ APPLICATION INFORMATION

● POWER ON

An initial pause of 500 μs is required after power-up and a minimum of eight (8) initialization cycle, (any combination of cycles containing a RAS clock such as RAS-only refresh) must follow an initial pause.

The VCC current (Icc) requirement of the HM4864 during power on is, however, dependent upon the input levels (RAS, CAS) and the rise time of VCC, as shown in Fig. 1.

● READ CYCLE

A read cycle begins with addresses stable and a negative going transition of RAS. The time delay between the stable address and the start of RAS-on is controlled by parameter tASR.

Following the time when RAS reaches its low level, the row address must be held stable long enough to be captured. This controlling parameter is tRAH. Following this interval, the address can be changed from row address to column address.

When the column address is stable, CAS can be turned on. The leading edge of CAS is controlled by parameter tRCD. The basic limit on the CAS leading edge is that CAS can not start until the column address is stable, and this is controlled by parameter tASC. The column address must be held stable long enough to be captured. The controlling parameter is tCAH. Note that tRCD (max) is not an operating limit of the HM4864 though its specification is listed on the data sheets. If CAS becomes on later than tRCD (max), the access time from RAS will be increased by the time which tRCD exceeds tRCD (max).

Following the time when CAS reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is tCAC -access time from CAS.

The access time from RAS -tRAC- is the time from RAS-on to valid Dout.

The minimum value of tRAC is derived as the sum of tRCD (max) and tCAC.

The selected output data is held valid internally until CAS becomes high, and then Dout pin becomes high impedance.

This parameter is tOFF.

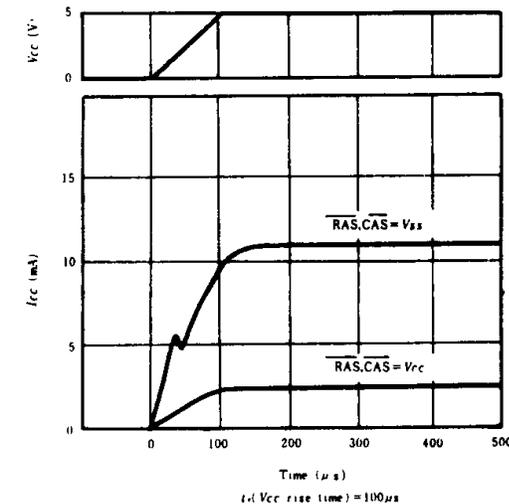
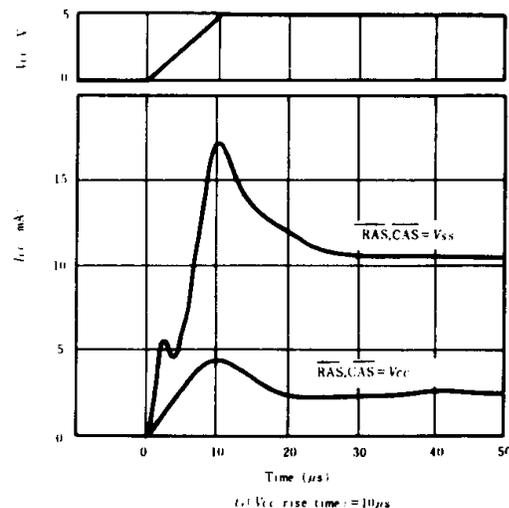


Fig.1 Icc vs. Vcc during power up.



● WRITE CYCLE

A write cycle is performed by bringing \overline{WE} low before or during \overline{CAS} -on.

Two different write cycles can be defined as:

Write cycle—Write data are available at the beginning of the \overline{CAS} -on so that the write operation starts at the beginning. In this mode, Dout and \overline{WE} signal times are not in any critical path for determining cycle time.

Following the time when \overline{WE} reaches its low level, \overline{WE} must be held stable long enough to be captured. This \overline{WE} -on pulse duration is called t_{WP} . The time required to capture write data in a latch is called t_{DH} . This cycle is called an "early write".

Read Write cycle—This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated.

\overline{WE} and Din are delayed until after Dout. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, Din and \overline{WE} become critical path signals for determining cycle time.

● CLOCK-OFF TIMING

\overline{RAS} and \overline{CAS} must stay on for Dout stabilized to valid data. In the case of \overline{CAS} , this is controlled by parameter t_{CAS} (min).

In the case of \overline{RAS} , this is controlled by parameter t_{CAS} (min). Following the end of \overline{RAS} , \overline{CAS} must stay off long enough to precharge internal circuits. The only parameter of concern is t_{RP} . Normally \overline{CAS} is not required to be off for minimum time of t_{CRP} . However, in a page mode memory operation, there is a t_{CP} (min) specification to control the \overline{CAS} -off time.

● DATA OUTPUT

Dout is three-state TTL compatible with a fan-out of two standard TTL loads.

When \overline{CAS} is high, Dout is in a high impedance state. When \overline{CAS} is low, valid data appears after t_{CAC} at a read cycle, and Dout is not valid as an early-write cycle.

● REFRESH

Refresh of the HM4864 is accomplished by performing a memory cycle at each of the 128 row addresses within each two millisecond time interval. A0 to A6 are refresh address pin compatible with standard 16K RAM (HM4716A, HM4816A). During refresh, either V_{IL} or V_{IH} is permitted for A7. Any cycle in which \overline{RAS} signal occurs refreshes the entire selected row. \overline{RAS} -only refresh results in substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

● PAGE MODE

Page mode operation allows faster successive memory operations at multiple column locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining \overline{RAS} at a logic low throughout all successive \overline{CAS} memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be decreased and the operating power is reduced. These are specifications.