National Semiconductor

DM54LS498/DM74LS498 Octal Shift Register

General Description

The LS498 is an 8-bit synchronous shift register with parallel load and hold capability. Two function select inputs (I_0, I_1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the input ($D_7 - D_0$) into the output register ($Q_7 - Q_0$). The HOLD operation holds the previous value regardless of clock transitions. The SHIFT LEFT operation shifts the output register, Q, one bit to the left; Q_0 is replaced by LIRO. RILO outputs Q_7.

The SHIFT RIGHT operation shifts the output register, Q, one bit to the right; Q_7 is replaced by RILO. LIRO outputs Q_0.

The output register ($Q_7 - Q_0$)—is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

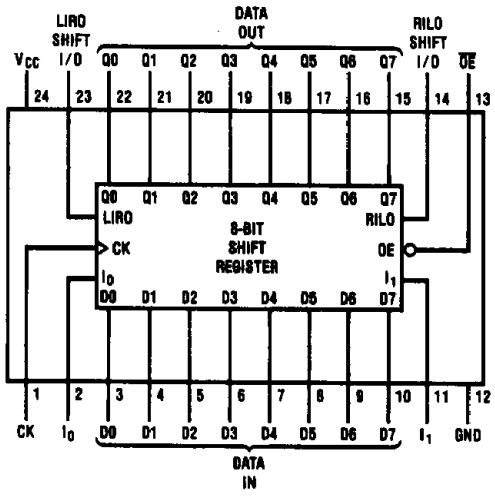
Two or more LS498 octal shift registers may be cascaded to provide larger shift registers as shown in the application section.

Features/Benefits

- Octal shift register for serial to parallel and parallel to serial applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP saves space
- TRI-STATE® outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

Connection Diagram

Top View



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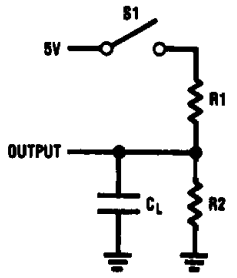
Order Number DM54LS498J, DM74LS498J or DM74LS498N
See NS Package Number J24F or N24C

Standard Test Load



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Function Table

$\overline{OE}$	CK	I_1	I_0	$D_7 - D_0$	$Q_7 - Q_0$	Operation
H	X	X	X	X	Z	HI-Z
L	↑	L	L	X	L	HOLD
L	↑	L	H	X	SR(Q)	SHIFT RIGHT
L	↑	H	L	X	SL(Q)	SHIFT LEFT
L	↑	H	H	D	D	LOAD

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65° to +150°C

Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55		125*	0		75	°C
t_w	Width of Clock	Low	40			35			ns
		High	30			25			
t_{su}	Set-Up Time		60			50			ns
t_h	Hold Time		0	−15		0	−15		

*Case temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IH}	High-Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN		I_I = −18 mA			−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = MAX		V_I = 0.4V			−0.25	mA
I_{IH}	High-Level Input Current	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum Input Current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OL} = 12 mA			0.5	V
			COM	I_{OL} = 24 mA				
V_{OH}	High-Level Output Voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = −2 mA	2.4			V
			COM	I_{OH} = −3.2 mA				
I_{OZL}	Off-State Output Current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output Short-Circuit Current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = MAX				120	180	mA

*No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

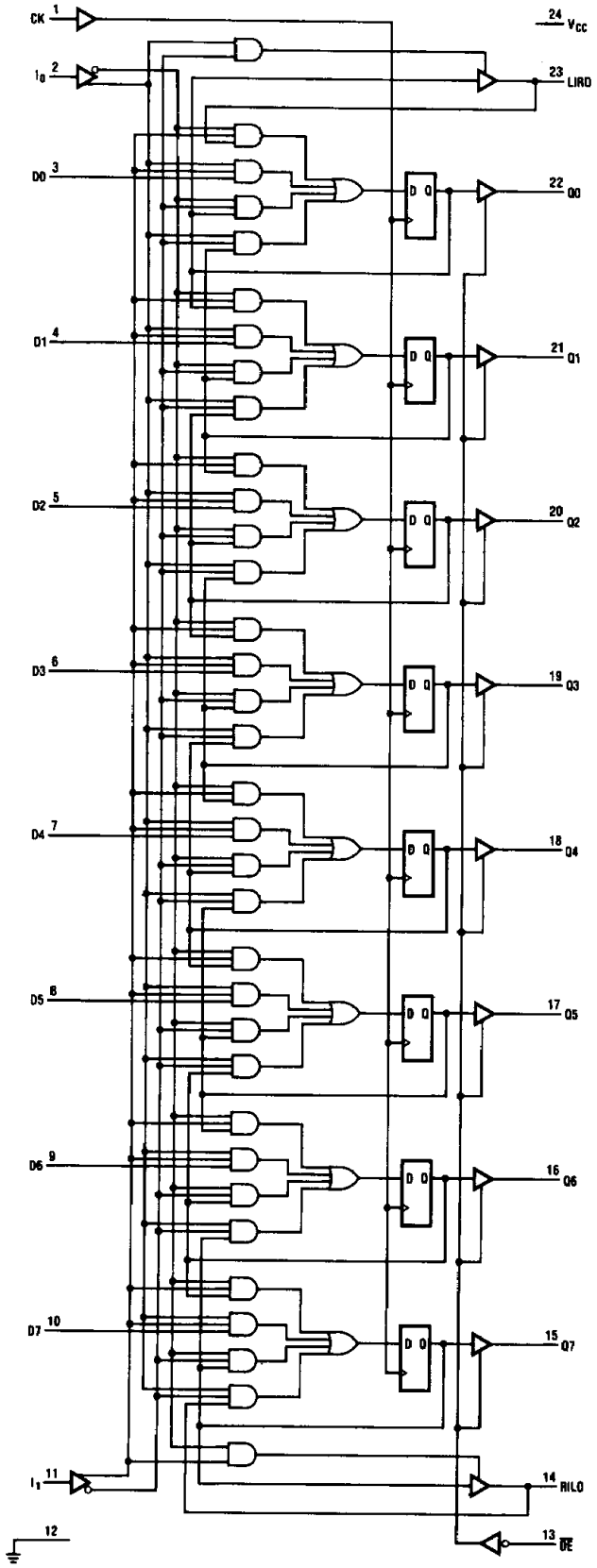
†All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Clock Frequency	C_L = 50 pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	I0, I1 to LIRO, RILO			35	60		35	50	ns
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PD}	Clock to LIRO, RILO			55	95		55	80	ns
t_{PZX}	Output Enable Delay			35	55		35	45	ns
t_{PXZ}	Output Disable Delay			35	55		35	45	ns

Logic Diagram

Octal Shift Register



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