Summary		HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
REG -> ALU -> FLAGS		185	317	60	99	50	82
1 Cycle BCD NMOS Flags	(Optional)	189	308	63	102	59	95
2 Cycle BCD CMOS Flags		118	199	40	65	35	56
REG -> ALU -> BREXIT		176	323	63	102	50	80
STPWAI -> NOP1 -> FETCHOP		118	234	50	82	50	82
REG -> ALU -> INC.DPH		142	244	50	79	50	79
REG -> INC16 -> REG		173	273	53	85	50	79
REG -> MEM R -> REG		143	230	51	75	48	68
Q -> ROM -> MIR		80	106	50	56	50	56
REG -> MEM W		120	236	44	72	44	72
Critical Path (2-Cycle BCD CMOS Flags)		185	323	63	102	50	82
Max Frequency (MHz)		**5.4**	3	**15.8**	10	**20.0**	12
Critical Path (1-Cycle BCD NMOS Flags)		189	323	63	102	59	95
Max Frequency (MHz)		**5.3**	3	**15.8**	10	**16.8**	10

Note: AC+ column includes TI CBT parts.

Note: AC propagation times are from Fairchild Datasheets (50pf, 25˚C, 5.0V) unless otherwise noted.

Note: HC propagation times are from TI Datasheets (50pf, 25˚C, 4.5V) unless otherwise noted.

Note: Target clocks rates: 2-cycle BCD CMOS Flags 20MHz, 1-cycle BCD NMOS Flags 16.36MHz for NTSC

Component Inventory	Component	Desc	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
	7400	NAND (PHL)	9.0	18.0	4.5	6.5	4.5	6.5
	7404	Inverter	9.0	19.0	4.0	7.0	4.0	7.0
	7408	AND	10.0	20.0	5.5	7.0	5.5	7.0
	7410	3-NAND	10.0	19.0	4.5	7.0	4.5	7.0
	7411	3-AND	10.0	20.0	4.0	8.0	4.0	8.0
AC N/A, use 74VHC27 (15pF, 5.0V)	7427	3-NOR	10.0	18.0	4.1	7.9	4.1	7.9
	7432	OR	10.0	20.0	5.5	7.5	5.5	7.5
	74161	Counter	25.0	41.0	5.0	9.5	5.0	9.5
	74138 AY	Decoder - A to Y	18.0	36.0	6.5	9.5	6.5	9.5
	74151 E	MUX - Enable to Y	15.0	25.0	6.5	10.0	6.5	10.0
	74151 S	MUX - Sel to Y	30.0	50.0	8.5	13.0	8.5	13.0
	74153 D	MUX - Data to Y	17.0	28.0	5.5	8.0	5.5	9.0
	74153 S	MUX - Sel to Y	21.0	30.0	6.5	11.0	6.5	11.0
(TI for HC, AC, AC+)	74238 AY	Decoder A to Y	17.0	30.0	8.8	13.6	8.8	13.6
	74245 E	Buffer Enable	23.0	46.0	5.5	9.0	5.5	9.0
(TI 74CBT3245 for AC+)	74245 T	Buffer TPD	15.0	21.0	3.5	6.5	0.25	0.25
(TI 74CBT3251 for AC+)	74251 D	MUX - Data to Y	17.0	39.0	7.0	11.0	0.25	0.25
	74251 S	MUX - Sel to Y	21.0	41.0	8.5	13.0	8.5	13.0
(TI 74CBT3257 for AC+)	74257 D	MUX - Data to Y	10.0	20.0	4.5	6.0	0.25	0.25
	74257 S	MUX - Sel to Y	10.0	20.0	4.5	6.0	4.5	6.0
	74273 S	Register - Setup	10.0	20.0	2.5	4.0	2.5	4.0
	74273 T	Register - TPD	15.0	32.0	5.5	10.0	5.5	10.0
(TI for AC)	74283 CC	ADDR CIN - COUT	23.0	39.0	10.3	16.0	10.3	16.0
(TI for AC)	74283 CS	ADDR CIN - S	27.0	46.0	10.3	16.5	10.3	16.5
(TI for AC)	74283 DC	ADDR Data to COUT	23.0	39.0	10.6	16.5	10.6	16.5
(TI for AC)	74283 DS	ADDR Data to Sum	25.0	42.0	10.6	16.5	10.6	16.5
	74541 E	Buffer Enable	17.0	30.0	6.0	8.5	6.0	8.5
	74541 T	Buffer TPD	12.0	23.0	4.0	6.0	4.0	6.0
	74574 E	Register - Enable	26.0	30.0	6.0	9.5	6.0	9.5
	74574 S	Register - Setup	10.0	20.0	0.0	1.5	0.0	1.5
	74574 T	Register - TPD	28.0	36.0	6.0	9.5	6.0	9.5
	74688 T	Comparator	22.0	35.0	22.0	35.0	22.0	35.0
	7474 S	Flip Flop Setup	10.0	20.0	1.0	3.0	1.0	3.0
	7474 T	Flip Flop TPD	20.0	35.0	5.9	10.0	6.0	10.0
	AT27C256R	ROM	45.0	45.0	45.0	45.0	45.0	45.0
	CY7C199CN	RAM	15.0	15.0	15.0	15.0	15.0	15.0

FLAGS

	Component	Desc	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
V Flag Evaluate	74151 S	MUX - Sel to Y	30	50	8.5	13	8.5	13
V Select	74251 D	MUX - Data to Y	17	39	7.0	11	0.25	0.25
			47	89	15.5	24	8.8	13
Z Flag Evaluate	7427	3-NOR	10	18	4.1	8	4.1	8
Z Flag Evaluate	7411	3-AND	10	20	4.0	8	4.0	8
Z Select	74251 D	MUX - Data to Y	17	39	7.0	11	0.25	0.25
			37	77	15.1	27	8.4	16
C.OUT	74251 D	MUX - Data to Y	17	39	7.0	11	0.25	0.25
C Select	74151 D	Decoder - A to Y	18	36	6.5	10	6.5	10
			35	75	13.5	21	6.8	10
N Select	74151 D	Decoder - A to Y	18	36	6.5	10	6.5	10
Max Flag			47	89	15.5	27	8.8	16

REG -> ALU -> FLAGS

A := A ADC B; SETF(NZVC)	Component	Desc	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74273 T	Register - TPD	15	32	5.5	10	5.5	10
R.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
A.R OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
LU	74153 S	MUX - Sel to Y	21	30	6.5	11	6.5	11
ADDR L	74283 DC	ADDR Data to COUT	23	39	10.6	17	10.6	17
SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
LSR.OUT	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
Max Flag			47	89	15.5	27	8.8	16
P Register	7474 S	Flip Flop Setup	10	20	1.0	3	1.0	3
			185	317	60	99	49.6	82
			23	40	7	12	6	10
			33	68	12	20	12	20

REG -> ALU -> BCD -> FLAGS

A := A ADC B	Component	Desc	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74273 T	Register - TPD	15	32	5.5	10	5.5	10
R.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
A.R OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
LU	74153 S	MUX - Sel to Y	21	30	6.5	11	6.5	11
ADDR L	74283 DC	ADDR Data to COUT	23	39	10.6	17	10.6	17
BCD.DETECT.LO	74151 E	MUX - Enable to Y	15	25	6.5	10	6.5	10
BCD.SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
BCD.DETECT.HI	74151 E	MUX - Enable to Y	15	25	6.5	10	6.5	10
BCD.ADJ.SEL	74153 S	MUX - Sel to Y	21	30	6.5	11	6.5	11
BCD.OUT	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
Register Write	74574 S	Register - Setup	10	20	0.0	2	0.0	2
Max Flag			47	89	15.5	27	8.8	16
P Register	7474 S	Flip Flop Setup	10	20	1.0	3	1.0	3
2 Cycle BCD CMOS Flags			118	199	39.6	65	34.6	56
2 Cycle BCD NMOS Flags			95	154	31.3	51	29.7	48
1 Cycle BCD CMOS Flags			236	397	79.1	130	69.1	113
1 Cycle BCD NMOS Flags			189	308	62.6	102	59.4	95

REG -> ALU -> REG

Note: MIR.SW switches to DPH := DPH + 1. Adds MIR.SW Enable time.

DPH := DPH + 1	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
NXT.CYCL B FF	7474 T	Flip Flop TPD	20	35	5.9	10	6.0	10
MIR.SW	74574 E	Register - Enable	26	30	6.0	10	6.0	10
R.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
DPH.R OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
LU	74153 S	MUX - Sel to Y	21	30	6.5	11	6.5	11
ADDR L	74283 DC	ADDR Data to COUT	23	39	10.6	17	10.6	17
SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
LSR.OUT	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
W->DPH	74541 T	Buffer TPD	12	23	4.0	6	4.0	6
DPH Register	74574 S	Register - Setup	10	20	0.0	2	0.0	2
			181	284	53.5	86	50.4	80

REG -> ALU -> BREXIT

PCL := PCL + B; EXIT.CC	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74273 T	Register - TPD	15	32	5.5	10	5.5	10
R.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
PCL.R OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
LU	74153 S	MUX - Sel to Y	21	30	6.5	11	6.5	11
ADDR L	74283 DC	ADDR Data to COUT	23	39	10.6	17	10.6	17
SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
C.OUT	74251 D	MUX - Data to Y	17	39	7.0	11	0.25	0.25
	7404	Inverter	9	19	4.0	7	4.0	7
BRANCH.EXIT	74251 D	MUX - Data to Y	17	39	7.0	11	0.25	0.25
	7410	3-NAND	10	19	4.5	7	4.5	7
NXT.CYCL B FF	7474 S	Flip Flop Setup	10	20	1.0	3	1.0	3
			176	323	63.1	102	49.6	80

STPWAI -> NOP1 -> FETCHOP

	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
IR	74273 T	Register - TPD	15	32	5.5	10	5.5	10
STPWAI.DETECT	7404	Inverter	9	19	4.0	7	4.0	7
STPWAI.DETECT	7411	3-AND	10	20	4.0	8	4.0	8
STPWAI.DETECT	7411	3-AND	10	20	4.0	8	4.0	8
STPWAI.DETECT	7408	AND	10	20	5.5	7	5.5	7
NOP1.DETECT	74151 E	MUX - Enable to Y	15	25	6.5	10	6.5	10
FETCHOP	7432	OR	10	20	5.5	8	5.5	8
NX.MX2	7432	OR	10	20	5.5	8	5.5	8
NXT.CYCL B FF	7404	Inverter	9	19	4.0	7	4.0	7
NXT.CYCL B FF	7410	3-NAND	10	19	4.5	7	4.5	7
NXT.CYCL B FF	7474 S	Flip Flop Setup	10	20	1.0	3	1.0	3
			118	234	50.0	82	50.0	82

REG -> ALU -> INC.DPH

DPL := B + Y; INCDPH.C	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74273 T	Register - TPD	15	32	5.5	10	5.5	10
R.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
Y.R OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
LU	74153 S	MUX - Sel to Y	21	30	6.5	11	6.5	11
ADDR L	74283 DC	ADDR Data to COUT	23	39	10.6	17	10.6	17
SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
INC.DPH	7400	NAND (PHL)	9	18	4.5	7	4.5	7
NXT.CYCL B FF	7410	3-NAND	10	19	4.5	7	4.5	7
NXT.CYCL B FF	7474 S	Flip Flop Setup	10	20	1.0	3	1.0	3
			142	244	49.6	79	49.6	79

REG -> INC16 -> REG

Note: Default Operand-fetch instruction - MIR.SW switches to load "0" in MIR. Adds MIR.SW Enable time.

B := DPL := *PC; PC += 1	Component	Desc	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
NXT.CYCL B FF	7474 T	Flip Flop TPD	20	35	5.9	10	6.0	10
MIR.SW	74574 E	Register - Enable	26	30	6.0	10	6.0	9.5
AD.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
PCH.ADL OE	74574 E	Register - Enable	26	30	6.0	10	6.0	10
INC2 ADDR	74283 CC	ADDR CIN - COUT	23	39	10.3	16	10.3	16
INC3 ADDR	74283 DS	ADDR Data to Sum	25	42	10.6	17	10.6	17
SKIP.ADR	74257 S	MUX - Sel to Y	10	20	4.5	6	4.5	6
S->PCH	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
PCH Register	74574 S	Register - Setup	10	20	0.0	2	0.00	2
			173	273	53.3	85	50.1	79

REG -> MEM R -> REG

Note: MIR.SW may switch back from DPH := DPH + 1. Adds MIR.SW Enable time.

PCL := *SP	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
NXT.CYCL B FF	7474 T	Flip Flop TPD	20	35	5.9	10	6.0	10
MIR.SW	74574 E	Register - Enable	26	30	6.0	10	6.0	10
AD.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
DPL.AD	7411	3-AND	10	20	4.0	8	4.0	8
DPL.AD OE	74541 E	Buffer Enable	17	30	6.0	9	6.0	9
RAM	CY7C199CN	RAM	15	15	15.0	15	15.0	15
ALU.BYPASS	74245 T	Buffer TPD	15	21	3.5	7	0.25	0.25
W->PCL	74541 T	Buffer TPD	12	23	4.0	6	4.0	6
PCL Register	74574 S	Register - Setup	10	20	0.0	2	0.00	2
			143	230	50.9	75	47.8	68

REG -> MEM W

*DP := X	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
MIR	74273 T	Register - TPD	15	32	5.5	10	5.5	10
AD.MX	74138 AY	Decoder - A to Y	18	36	6.5	10	6.5	10
DPL.AD	7411	3-AND	10	20	4.0	8	4.0	8
DPL.AD OE	74541 E	Buffer Enable	17	30	6.0	9	6.0	9
Must be ok at half-cycle			60	118	22.0	36	22.0	36
Symetrical Full Cycle			120	236	44.0	72	44.0	72

Q -> ROM -> MIR

MIR := ROM[Q]	Component	Description	HC Typ	HC Max	AC Typ	AC Max	AC+ Typ	AC+ Max
Q.REG	74161	Counter	25	41	5.0	10	5.0	10
ROM	AT27C256R	ROM	45	45	45.0	45	45.0	45
MIR	74574 S	Register - Setup	10	20	0.0	2	0.0	2
			80	106	50.0	56	50.0	56