*WHITE PAPER*

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# SRAM Board Design Guidelines

## *Abstract*

This white paper examines several important board design considerations to help an engineer while designing with Cypress SRAMs.

## *Introduction*

The simple smart electrical engineering practices mentioned in this document help in excellent long-term system performance if implemented properly.

This white paper covers the following topics.

- Decoupling capacitors
- Printed circuit board (PCB) issues
- Terminations

## *Decoupling (Bypass) Capacitors*

Decoupling capacitors, commonly referred to as bypass caps, are often the most confusing component in a high-speed digital design. Although engineers know that capacitors must be in the design, the purpose and operation of the part may be unclear. Additionally, as the speed of signals increases, many older designs using the same decoupling methodology must be updated.

Simply put, the reason that systems need decoupling capacitors is to reduce the amount of noise in the power system. More specifically, the goal of this capacitor is to eliminate the effects of inductance on the power supply bus. Essentially, the capacitor, which has a low series resistance and series inductance, decouples or “bypasses” the power supply bus from the integrated circuit (IC).

The decoupling capacitor has three major purposes:

- Isolates the circuit from unwanted ripples on power and ground pins.
- Gives a low-impedance path from the power plane to the ground plane.
- Gives a signal return path between the power and ground planes.

## *The Problem with Inductance—Ground Bounce*

An important function of the decoupling capacitor is to eliminate the effects of inductance. But why is inductance a big problem? To examine how big a problem the wiring inductance can be, consider this equation.

$$V = (\frac{dI}{dt}) \times L \qquad \text{Equation 1}$$

This equation states that a change (or surge) in the current taken across a finite inductance will cause an increase in voltage. Generally, when an IC is in static mode, the wiring inductance is not a problem. With the device’s outputs not switching, the current being drawn by the device does not change, and there is no additional voltage (noise) on the power lines. When the outputs of the IC switch, however, there will be a surge in current as the IC attempts to drive its loads to a higher or lower voltage level. This surge in current may cause significant noise to be added to the power lines.

Consider Figure 1, which shows the simplified schematic of an SRAM output. The inductors that are shown represent the wiring inductance between the

die of the device and the power plane. The output goes to a high voltage level when transistor Q1 is on and transistor Q2 is off. The output is tied to ground and a low voltage level when Q2 is on and Q1 is off.

At the moment that Q2 turns on and Q1 turns off, a spike of current flows from the output to the ground, through transistor Q2. This changing current also flows through the intrinsic and wiring inductance shown and, according to Equation 1, changes the voltage at Reference B. In other words, as Q2 turns on and the voltage at the output begins to drop, the voltage at Reference B (which, ideally, would be zero volts) will actually rise because of the current spike. For this reason, the output voltage $V_{OUT}$ does not fall all the way to zero as it should, but rather "bounces" above a grounded voltage level. This is what is known as 'ground bounce.' A similar result occurs at Reference A when Q1 switches on and the current spike drives the output high. In this case, the ending value of $V_{OUT}$ will be below $V_{DD}$. This effect is called "voltage droop."

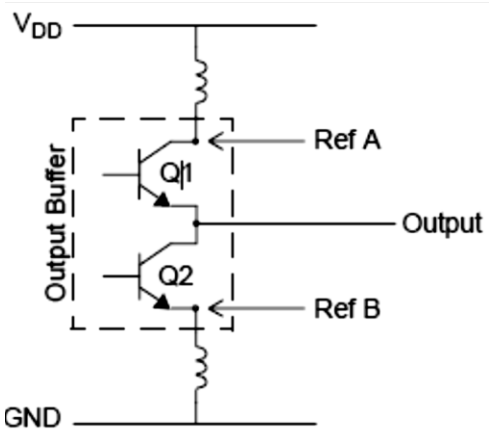


**Figure 1. Effects of Ground Bounce**

## *Choosing the Right Capacitor Value*

To decrease the problems of ground bounce and voltage droop, decoupling capacitors should be connected between each power pin on a device and ground. The initial capacitance value that is chosen gives a minimum current need. When the output buffers of an SRAM switch, the power terminals will sag because of the effects described previously. The function of the decoupling capacitor is to supply this momentary need in current with its stored charge. To do this, it must store a minimum amount of energy. The buffer loading determines this energy. The amount stored is given by this formula:

$$Q = CV \qquad \text{Equation 2}$$

Where,

Q = Charge stored

V = Applied voltage

C = Bypass capacitance

Differentiating this equation yields,

$$I(t) = \frac{dQ}{dt} = C \times \frac{dV}{dt} \qquad \text{Equation 3}$$

You can use this equation to calculate the capacitance needed to prevent the voltage drops from the switching output drivers. For example, suppose you have an SRAM with eighteen 3.3-V output drivers driving a 50-ohm trace with a rise and fall time of 3 ns. Assume, also, that a voltage drop of 300 mV is the maximum amount of voltage drop allowable to the component.

First, you must calculate the output current during the rise of the clocks. Assuming the outputs reach 3 V, each output requires 3 V/50 ohm = 60 mA. Because the SRAM has eighteen such drivers, the total current required is 1080 mA. Solving for C in Equation 3 gives the following:

$$C = I \times \left( \frac{dt}{dV} \right)$$ Equation 4

$$C = 1080mA \times \left( \frac{3ns}{300mV} \right) = 0.0108\mu F$$ Equation 5

This result suggests that this amount of total capacitance is required on the component to maintain less than 300 mV of voltage swing. Often, 0.1 µF capacitors are used for bypassing at board level. Another way to view this situation is to say that a 0.1 µF capacitor supplies 1080 mA of instantaneous current in 3 ns with only 32.4 mV of voltage swing across the bypass capacitor.

This example assumes a worse-case scenario voltage swing on the outputs of 3 V. Depending on the termination method used, this swing could be less than this amount. However, because this is used only as a guide, it is best to overestimate the value.

### *Capacitor Filtering*

You have seen that the main role of decoupling capacitors is to block unwanted noise going onto and coming from the power plane. However, decoupling caps are more than just a capacitor. Because capacitors always have a finite, intrinsic resistance and inductance, they are, in effect, a capacitor in series with an inductor and a resistor, as shown in Figure 2.

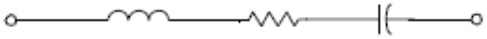

**Figure 2. Capacitor Model**

This concept is important in understanding what happens during the operation of a capacitor. Consider Figure 3, which shows the behavior of two ideal components, a capacitor and an inductor, which represent the reactive parts of the capacitor shown in Figure 2. Without any lead inductance or resistance, the resulting capacitive reactance approaches zero with increasing frequency. You can see that the inductive reactance of the ideal inductor, without any stray capacitance, approaches infinity.

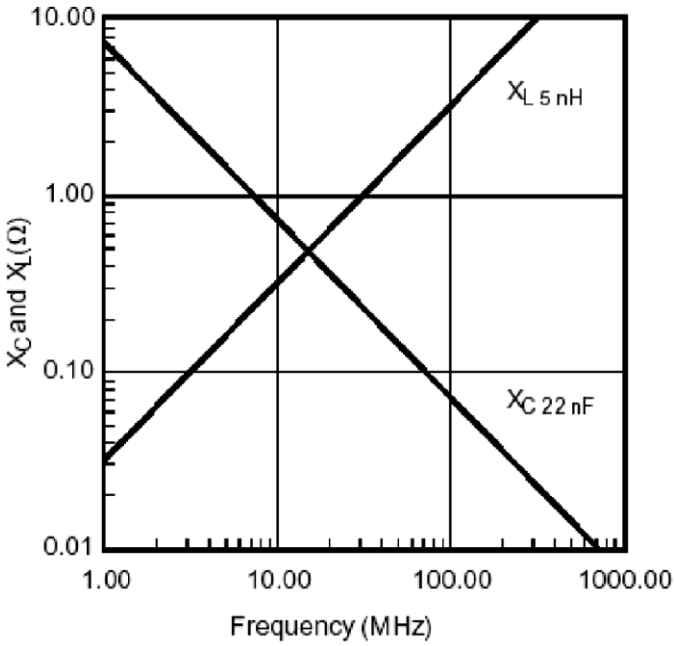


**Figure 3. Z vs. f for Parts of a Real Capacitor**

The impedance curve of “real” capacitors resembles the traces marked 22 nF and 100 pF in Figure 4. The shape of these calculated curves match those in a capacitor manufacturer’s datasheets. This means, in a circuit, that a capacitor acts as a low-impedance element over only a limited range of frequencies. To extend this frequency range, many references propose adding a second capacitor to bypass frequencies outside the limited range of the single capacitor. This approach expects a resulting impedance curve such as the solid line marked “Expected” in Figure 4. This solution, however, is not mathematically sound and has a significant problem at intermediate frequencies.

The actual occurrences when two capacitors of different values are in parallel are shown in Figure 5. Notice the spike in impedance just above 100 MHz. The goal of obtaining lower impedance across a wider frequency is not achieved. On the contrary, the impedance has actually increased in some areas. For this reason, the practice of using two different valued capacitors to decouple a power supply bus is not recommended.

However, one method will help to lower the impedance across all frequencies. When two capacitors of the same value and package size are in parallel with each other, no peak increase in impedance is achieved. But they do have the effect of decreasing the inductance by half. Figure 5 shows that adding additional capacitor introduces two low impedance nodes. Addition of more capacitance will result in flattening of the impedance curve. This is a recommended practice, although it may be constrained by available board space. In next section we will evaluate the band of frequencies which needs to be bypassed.

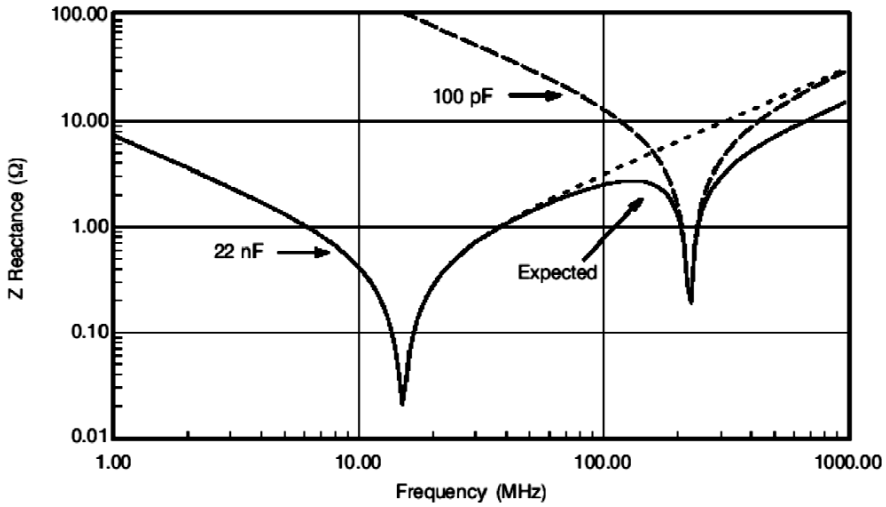


**Figure 4. Expected Impedance of “Real” Capacitors**

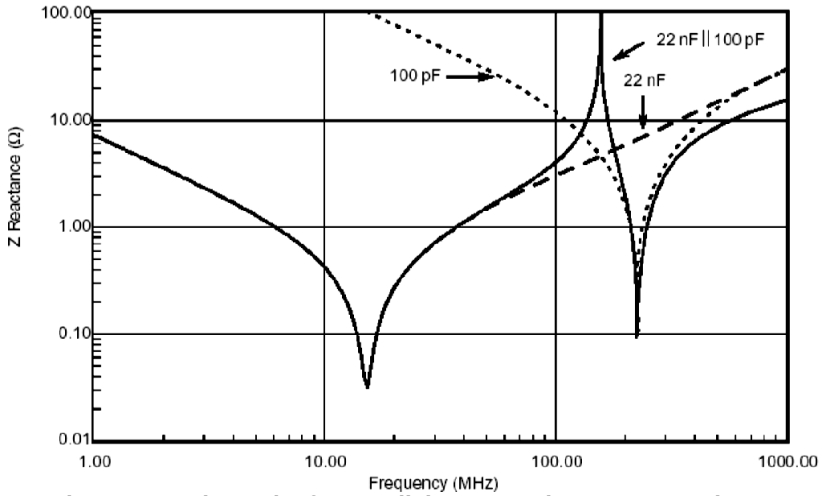


**Figure 5. Real Z and F for Parallel 22-nF and 100-pF Capacitors**

### *Which Frequencies to Bypass*

The highest frequency for which the board-level bypass capacitor is effective for bypassing supply noise is determined by its series inductance. The board-level bypass is used to bypass supply noises at frequency higher ($f_{BYPASS}$) than the frequencies not bypassed by the power supply bulk capacitance. Yet the board-level bypass is usually too large to bypass frequencies higher than $f_{BYPASS}$. In previous section we arrived at a board-level bypass capacitor of value 0.1 µF. If you use a surface mount chip capacitor, typical series inductance ($L_{series}$) will be around 1.5 nH. If you want to achieve target impedance ($Z_{max}$) of 0.1 Ohms for the bypass capacitor structure then $f_{BYPASS}$ will be calculated as per equation 6.

$$f_{BYPASS} = \frac{Z\max}{2\Pi Lseries} = 10MHz \qquad \text{Equation 6}$$

It is a common misconception that faster clock rates create a need for higher frequency decoupling. This is only partly true. Because the frequencies have increased, the technology for high-speed memories has been driven to provide faster rise and fall times. Therefore, a signal with a frequency of 1 MHz needs the same decoupling as a clock running at 50 MHz using the same high-speed buffers. The difference may be that there is more timing margin afforded in the slower speed system. A rough generalization suggests that frequencies up to one-half the fastest signal transition rate (rise or fall) frequency must be bypassed:

$$f_{KNEE} = \frac{0.5}{Transitionrate} = 167MHz \text{ for Transition rate of 3 ns} \qquad \text{Equation 7}$$

Most energy in digital pulses concentrates below the knee frequency and that the behavior of a circuit at the knee frequency determines its response to digital pulses. Therefore, behavior of the circuit at frequencies above the knee frequency has minimal effect on digital performance. From equations 6 and 7, we observe the bypass capacitor must have a nearly flat impedance curve between 10 MHz to 167 MHz. This result in an upper limit of the total inductance ($L_{max}$) this capacitor structure can have at highest frequency of interest ($f_{KNEE}$). As a single capacitor cannot have low impedance over a wide frequency band, an array of bypass capacitors is used.

$$L_{MAX} = \frac{Z_{MAX}}{2\Pi f_{KNEE}} = 95pH \qquad \text{Equation 8}$$

With typical $L_{series}$ of around 1.5nH, we can calculate total number of capacitors arrays needed using equation 9.

$$N = \frac{Lseries}{L\max} = 15.7 \approx 16 \qquad \text{Equation 9}$$

The total array bypass must have impedance less than $Z_{max}$, even at the lowest frequency $f_{BYPASS.}$ So the total array bypass capacitance is determined as follows:

$$C_{array} = \frac{1}{2\Pi fBYPASS * Z\max} = 159nF \qquad \text{Equation 10}$$

The individual elements ($C_{bypass}$) array bypass will be determined as follows:

$$C_{bypass} = \frac{C_{array}}{N} = \frac{159nF}{15.7} = 10.1nF \qquad \text{Equation 11}$$

From this calculation, in order to minimize the effects of series inductance in the bypass capacitors, you must distribute sixteen 10 nF capacitors around the board. Adding so many capacitors will generally not be possible due to space or cost constraints. Based on these constraints, designers can chose to add sufficient number of capacitors, which are permissible along with the board-level bypass capacitor.

You can see that decoupling is actually a four-part system that consists of the power supply, bulk capacitors, decoupling capacitors, and intrinsic capacitance in the board. Each provides decoupling in its respective frequency bands with the power supply addressing the very low frequencies and the intrinsic board capacitance addressing the high frequencies. The difference between the capacitance is large enough between each part that the large spiking effect with multiple capacitor value interaction explained previously does not occur. However, between each frequency band there will be small peaks. These peaks will always exist, although they can be moved slightly.

Generally, engineers have limited ability to change the characteristics of the power supply and board plane capacitance. But it is possible to vary the bulk and decoupling capacitance values. The goal is to have the four-part system provide a low impedance path (less than 1 ohm) throughout the frequency range. By adjusting the values of the decoupling capacitors, the small impedance peaks can be shifted to allow for the lowest impedance in the frequency ranges of concern.

### *Decoupling Capacitors: Design Recommendations*

As you have now seen, decoupling capacitors play a major role in how well the SRAM performs. Along with appropriately choosing the correct value capacitor, connecting them on the board is of extreme importance in terms of performance. Generally, a PCB should be designed to keep wiring and lead inductances as low as possible. Long, narrow PCB traces should be avoided because they increase inductance. Passing through a via is acceptable provided the path is lower inductance than an alternative longer trace. The following is a list of rules to follow when designing with decoupling capacitors.

- Use only one value capacitor for the component.
- Keep decoupling capacitors as close to the component as possible.
- Use at least one capacitor on each power pin.
- Keep capacitors on the same side of the board as the component, if possible.
- Minimize the lead and wiring inductance.

Make sure that the capacitor value meets the voltage swing requirements, and that it gives a low-impedance path to ground in the intended frequency range of the application.

## *PCB Layout Considerations*

The PCB contributes two significant functions in an electrical design: mechanical locations for the components that reside on the board, and connectivity between components. These connections play an important role in generating a solid pathway to the power system and ensuring the highest degree of signal integrity.

The traces and planes that make up a printed circuit board can be separated into two categories:

- Pathways for the power source.
- Traces needed to carry the actual signals.

This section examines how both of these directly affect system integrity.

### *Power and Ground Planes*

Power planes are large sheets of a conductive material that typically reside on entire PCB layers. They provide four primary functions to the circuit:

- A low-impedance path for power from its source to the components on the PCB.
- A physical channel to vent and move heat from the components.
- Electrostatic shielding between the electromagnetic fields of signal traces that run on both sides of the planes.
- A sheet capacitance for the ground plane that exists on other layers of the PCB. This, in turn, gives additional AC bypassing within the power circuitry of the PCB.

The primary functionality of a power plane is to reduce the resistance that causes a voltage drop between component and power source. The thickest power plane available will give the best results. For example, using a two-ounce copper power plane instead of a one-ounce plane will cut in half any point-to-point path resistance. It can be thought of as having two resistors (and inductors) in parallel. The increased plane thickness reduces both the DC resistance and AC inductance drops. The drop in DC resistance allows the power supply to reach the component cleanly, while the reduction in AC inductance provides a low-impedance path for signal return currents.

As a secondary benefit, the thicker plane also increases the ability to sink heat out of the component. The bond wires and lead frames are a major thermal path in nonheat-sinked components.

The planes also help decrease electromagnetic interference (EMI). They provide a lower-impedance path across which the EMI develops and a larger faraday shield to short out these radiated fields.

The sheet capacitance (also known as plane capacitance) that the power plane provides is proportional to its size, its distance from the ground plane, and the dielectric constant of the material between them. It has the benefit of providing bypass capacitance, particularly at high frequencies. Although it does not come close to supplying all of the bypassing needs of a high-speed logic design, it should be used to its maximum. The capacitance of the planes can be calculated with this equation:

$$C = 0.225_{E_R}\left(\frac{[(N-1)\times A]}{t}\right)$$

Equation 12

Where,

$E_R$ = Relative dielectric constant

N = Number of plates

A = Area of one side of one plate in square inches

t = Thickness (separation of plates) in inches

For example, if you use a 10-inch by 10-inch FR-4 board with an $E_R$ of 4.1 and 0.005-inch separation between the power and ground plane, the capacitance is calculated as

$$C = 0.225(4.1)\left(\frac{[(2-1)\times 100]}{0.005}\right) = 18,450pf$$

Equation 13

This is equivalent to 184 pF per square inch. Table 1 shows the dielectric constants for several common materials used in PCB design today. You should always consult your fabricator for the precise ER value, because different epoxies are used when constructing a PCB. Dielectric constants of PCBs also change with frequency, as shown in Table 1.

**Table 1. Dielectric Constants**

| Material | $E_R$ | |
|---|---|---|
| | At 1 MHz | At 300 MHz |
| FR-4, Tetra Functional | 4.2 to 4.6 | 4.0 to 4.3 |
| FR-4, High-grade Multifunctional | 4.2 to 4.6 | 4.1 to 4.4 |
| Polyimide | 4.2 to 4.6 | 4.1 to 4.3 |
| GETEK | 3.9 to 4.1 | 3.9 to 4.0 |
| BT | 3.6 to 4.1 | 3.55 to 4.0 |
| CE | 3.6 to 4.0 | 3.6 to 4.0 |

### Vias

Vias are commonly used to connect the power plane to the power traces that ultimately attach to the power pins of the components. They can also have an impact on the power signal quality.

First, vias produce a higher resistance than a copper trace. This is because plated granular copper is typically used in the fabrication of the via. The resistance of a via changes based on the thickness of the copper that is plated in the via hole. Therefore, larger vias have a lower DC resistance and, for this reason, develop less of a DC voltage drop for any given current.

Vias also add inductance to the power trace. A positive feature of this inductance is that it causes high-frequency noise that is present on the power plane to stay on the plane. Unfortunately, the inductance isolates the capacitance effect of the power plane from the components on the other ends of the vias. Filling vias with solder, using heavy plating, enlarging their size, and using multiple vias for each power connection are the preferred methods of lowering both the resistive and inductive parasitic effects they have on power connections.

**Power Traces**

Similar to vias, a trace also has some amount of resistance, capacitance, and inductance. The overall resistance must be kept to a minimum to avoid voltage drop on the trace. For the power plane to reach the power trace and ultimately the component, a via is also required.

If connections to the device are made in the correct sequence, the resistance and inductance of the trace and via keep the component's noise from passing into the power plane. This effect increases as the frequency of the noise rises. To achieve this isolation, the power trace must pass from the via to the decoupling capacitor's pad and then to the component. This order is important to create an island of protected trace between the decoupling capacitor and the component.

The trace between component and bypass capacitor must be as short as possible. As mentioned previously, the goal is to keep the inductance between the devices to a minimum. A short, wide trace will produce better results than a long, narrow trace.

**Signal Return Paths**

The power planes play a key role in the return currents of high-speed digital signals. At very slow speeds, the return current follows the path of least resistance. At higher speeds, however, the return currents follow the path of least inductance. This can be on either power or ground plane, directly below the signal trace. Normally, the return path is on the ground plane on standard PCB designs. When the return current reaches the driving component, the decoupling capacitors supply the bridge to the proper voltage plane. To maintain good signal integrity and to minimize crosstalk, a clean, unobstructed return path must be provided. For example, if a return signal encounters a 5-ohm trace within the ground plane, the integrity of the normal signal on the 50-ohm trace can be compromised.

There are a few simple rules to follow for planes. First, a plane should be as continuous as possible. Excessive clearances around holes that pass through may make fabrication easier, but it can cause the return current to travel through a non-optimal path. The effect of the clearance holes should be analyzed. Second, cutouts in the ground plane must be avoided. Similar to the clearance holes for the vias, a ground plane cutout will force the return path current around the cutout if the signal trace crosses above the cutout. This will increase the inductance of the path and decrease the rise time of the digital signal on the trace. It will also increase the potential for crosstalk.

**Crosstalk**

Crosstalk can exist between traces on a PCB. If this occurs on an input signal to the SRAM with sufficiently strong amplitude, a false trigger can occur. Crosstalk should therefore be minimized in the design.

As a signal travels through a trace, it creates a magnetic field. It also reacts to other magnetic fields within its path. These magnetic fields have adverse effects on digital signals because they create unwanted noise on other signals. This effect is known as *crosstalk.* The voltages that external fields cause are proportional to the strength of the external fields and the length of the trace that is exposed to the field. Often, the trace that causes the crosstalk is termed the "source" or "aggressor," and the trace that is affected first is called the "victim."

Crosstalk between traces is a function of both mutual inductance and mutual capacitance. A model of inductance and capacitance between traces is shown in Figure 6. Its magnitude is proportional to the distance from the source trace, the speed of the signal edge rate, and the impedance of the victim trace. In digital systems, crosstalk caused by mutual inductance is typically equal to or larger than the crosstalk associated with mutual capacitance.

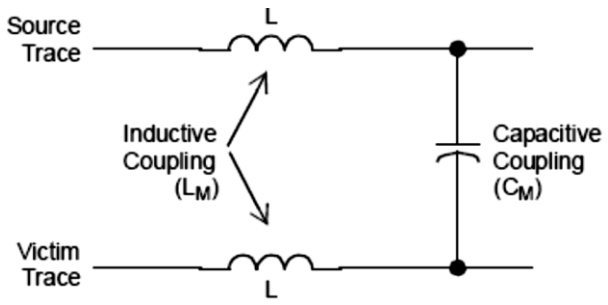


**Figure 6. Mutual Coupling between Traces**

To illustrate the effects of spacing, the mutual inductance LM can be calculated with this equation:

$$LM = \frac{L}{\left(1+\left(\frac{s}{h}\right)^2\right)}$$

Equation 14

Where,

L = Inductance of the wire

s = Separation between the wires

h = Height above the plane

This shows that by moving the traces away (value s) from each other or by moving the traces closer (value h) to the plane, the mutual inductance is reduced by the square of the charge. And, because crosstalk is proportional to the mutual inductance, the magnitude of the crosstalk is also reduced. Figure 7 illustrates this model.

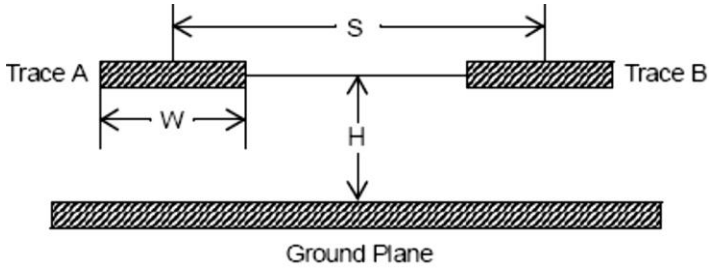


**Figure 7. Trace and Ground Planes**

The mutual capacitance CM injects current $I_M$ into the victim trace and can be calculated as:

$$I_M = C_M \times \left(\frac{dV_S}{dt}\right)$$

Equation 15

Where, $dV_S = V_S$ is the source voltage

Figure 8 illustrates the effects of trace impedance on crosstalk coupling. The higher the impedance of the victim trace, the more susceptible it is to noise from crosstalk. Figure 9 shows a similar effect but with varying the width of the trace line. Wider traces produce less crosstalk coupling. Therefore, minimum coupling is created with maximum spacing, maximum trace widths, and minimum impedance.

To minimize the effects of magnetic field coupling, three basic rules should be followed.

First, separate the traces with more distance. The effect that is seen is directly proportional to the square of the distance of the elements. Doubling the distance reduces the coupling by a factor of four.

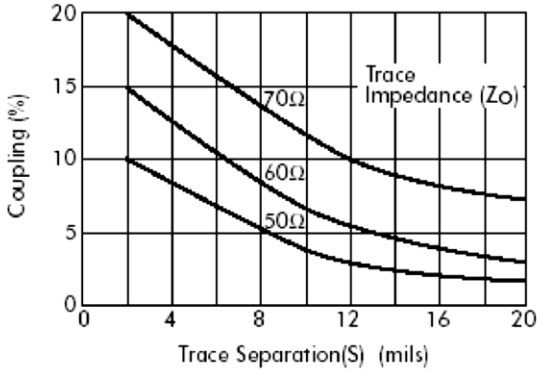


**Figure 8. Crosstalk versus Impedance and Spacing**

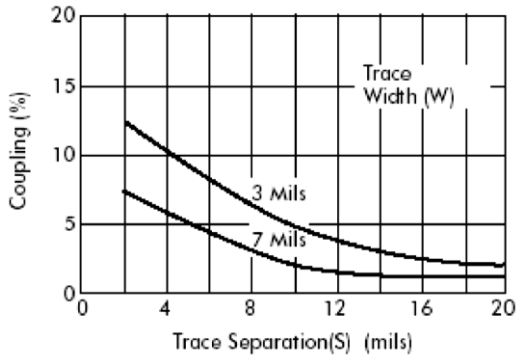


**Figure 9. Crosstalk versus Width and Spacing**

The second method of decreasing the coupling is to shield the target trace. Either routing it on another layer or placing protective guard traces between the two does this. In this way the magnetic lines will have a portion of their energy developed in the protective traces, usually at ground potential, and the field that cuts across the trace being shielded is less.

A third way to reduce the impact of crosstalk is to use differential signaling. This type of signal rejects noise from crosstalk, if both true and complement signals are equally affected. This is commonly called common-mode noise rejection. However, if the crosstalk affects one trace of the differential pair and not the other, noise coupling can be a factor.

**Layers**

To keep noise at a minimum and to achieve the best in signal integrity, control of the PCB layers is necessary. As was mentioned, spacing power and ground planes close together gains additional bypassing capacitance. Of more importance is the creation of a reference plane that provides constant trace impedance. The reference plane is usually the ground plane. The thickness of the substrate between controlled impedance traces and the ground plane must be selected to be both manufacturable and able to keep the desired characteristic trace impedance within acceptable limits. As the spacing of layers decreases, the ability to hold tight, repeatable spacing value decreases. A 1-mil variation on a 10-mil spacing is 10%; on a 20-mil spacing it is only 5%. You should consult with your manufacturer on the tolerances.

When power planes are correctly bypassed, they are at the same AC potential as ground planes. Therefore, they can be used as a reference for controlled impedance traces. Using both power and ground planes for same signal, however, is unwise because the transition between the two has a high potential for causing noticeable impedance discontinuities in trace impedance, which is a source of unwanted reflections (described in a subsequent section).

**Vias in Traces**

When routing a trace, the signal should remain on the same signal plane. Using vias to route to another plane diminishes signal quality. Vias should therefore be avoided as much as possible. If vias must be used in a high-speed design, consider the following guidelines:

- Make vias as large as possible (more area equals less inductance and resistance).
- Plate external layers with the maximum thickness of copper during fabrication.

## *Reflections and Terminations*

Another problem that arises in digital signal systems involves reflections because of poorly terminated transmission lines. This section discusses a few important points to remember when designing with long wiring networks.

**What is a Reflection?**

A reflection is an unwanted pulse on a transmission line that is a result of an unmatched source or load impedance. The transmission line has an intrinsic value called its characteristic impedance. A reflection back toward the driver source can occur if the line's load and characteristic impedances are not matched. A second reflection back toward the load can occur if the source and characteristic impedances are also not matched.

**Why do Reflections Occur?**

Reflections occur because of impedance mismatches that cause a disproportion of energy transfer. If the line is ideal, and the source impedance $Z_S$ equals the load impedance $Z_L$, then half the energy in the propagating signal will be lost in the source impedance, and the other half in the load impedance (because the ideal line is lossless). However, if the load resistor at the end of the line is larger than the line's characteristic impedance, there will be extra energy available that is "reflected" back toward the source. That is, there is another signal that propagates down the line that "bounces" off the load if there is an impedance mismatch.

**Characteristic Impedance**

The most important variable of any line is its characteristic, or input, impedance. This is the impedance seen looking into the two left-side terminals of the line.

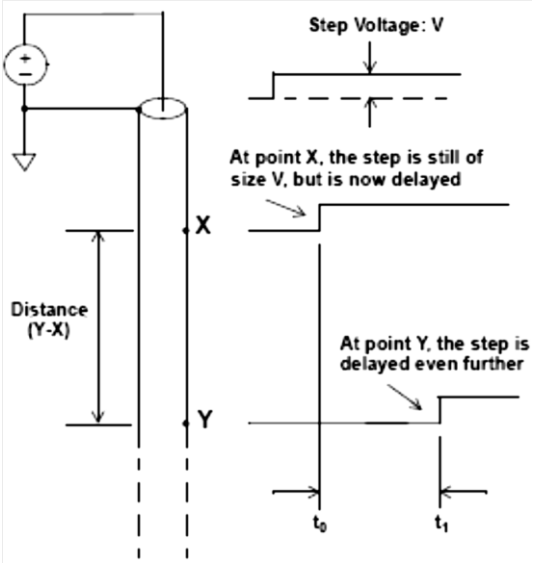


**Figure 10. Voltage Step Input to an Ideal Line**

Figure 10 illustrates how a digital pulse propagates down an ideal line. The pulse is set onto the beginning of the line by the source at time t = 0. This pulse is then transferred down the line without being distorted or attenuated while it is delayed in time according to the line's propagation delay. At point X, the voltage on the line is low, until time $t_0$ at which time the signal passes point X on the line, and we can see that the pulse drives the voltage up to the high level. A similar situation exists for point Y, except that the signal stays low longer while it waits for the pulse to propagate down the line.

We can find the characteristic impedance of this line by finding the amount of current it takes to impress the step voltage on a given length of the line, in this case between arbitrary points Y and X.

The capacitance of the length of line between points X and Y is given as:

$$C_{XY} = \left(\frac{C}{in}\right) \times (Y - X)$$

Equation 16

The total additional charge necessary to charge the capacitance between these points is equal to:

$$\text{Charge} = Q_{XY} = \left(\frac{C}{in}\right)(Y - X)V$$

Equation 17

The time interval (in seconds) during which $C_{XY}$ must be charged is equal to the separation of the two points times the propagation delay in seconds per unit length:

$$T = (Y - X)\sqrt{\left(\frac{L}{in}\right)\left(\frac{C}{in}\right)}$$ Equation 18

The average current supplied is equal to the total charge supplied divided by the length of time T:

$$I = \frac{\text{Charge}}{T} = \frac{\left(\frac{C}{in}\right)(Y - X)V}{(Y - X)\sqrt{\left(\frac{L}{in}\right)\left(\frac{C}{in}\right)}}$$ Equation 19

This gives us the current flow required to sustain a propagating step edge of V volts. Therefore, the characteristic impedance of an ideal line can be found through simplification.

$$Z_o = \frac{V}{I} = \sqrt{\frac{L}{C}}$$ Equation 20

Where, L and C are given in per-unit lengths.

As this equation shows, the value of characteristic impedance for ideal lines is real-valued, constant, and dependent only on the inductance and capacitance of the line-per-unit length. This allows us to model a transmission line as a simple resistor.

The characteristic impedance equation given above for an ideal line does not depend on the frequency of the system. This is not the case for a lossy line, however. The general formula for characteristic impedance is given as,

$$Z_o = \frac{V}{I} = \sqrt{\frac{R + j\omega L}{j\omega C}}$$ Equation 21

This is the impedance if a finite value of resistance exists. Note that $Z_o$ is actually a function of frequency. However, because digital signals operate at very high frequency along PCB traces that have very low resistance, it is simpler to use the form given in Equation 15

**Termination Strategies**

The end goal of all termination strategies is to remove voltage reflection on the line by cancelling out the two voltage reflection coefficients. There are two general strategies for doing this:

- Match the load impedance to the line's characteristic impedance.
- Match the source impedance to the line's characteristics impedance.

Under one of these conditions, the load or source reflection coefficient will be made to equal zero and there will be no reflection. If the load is matched, there will be no reflection back to the source; if the source is matched, this reflection will not bounce back again toward the load. Matching the load is slightly preferred, because eliminating the first reflection will reduce EMI and electrical noise. Also, it seems logical to try and eliminate any reflections as soon as one might occur.

## Summary

This white paper describes the role of bypass capacitors in suppressing supply and ground noise due to transient currents drawn by switching transistors. It also explains ways to find the right bypass capacitors for any design based on the transition time, provides layout guidelines on how the power supplies and signals can be routed for better power and signal integrity, and analyses sources of reflection and how terminations can be used to minimize them.

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