Reset Circuit
(U4A)

Clock Generator (X1, U5A/B)
8Mhz and synchronous 2Mhz
50% duty cycles

RD/WR Demux (U2A/B, U4B)
Gates separate /RD and /WR signals

Address Decoder (U3, U6A/B)
8x 8kbyte (0x2000) windows
VRAM enables also RAM or ROM

Output Port
Strobed byte wide output port
to FTDI FT245 module for
debug output

NOP Generator (U13)
D7 Lo=0b11101010 0xEA (NOP)
D7 Hi=0b01100000 0x60 (RTS)
0b01000000 0x40 (RTI)

ROM Address MUX (U17,18,19,U2C,U4D)
Selects AB when reading ROM
or ROW counter and Char ROM
when NOP generator active

Logic supply & Decoupling
Each IC has minimum 100nF cap &
Complex ICs also have 1uF Tant

Mono PAL video output
1V p/p 75 Ohm

Video Serializer/Inversion/Blank (U23,U22,U1A)
U22A Enables Video on first NOP generator, blanking on RTS
U22B/U1A inverts each charatcter based on D5
U23 serializes byte at 8MHz Dot clock

DB Buffers (I12,U20)
U20 Disconnects ROM DB
when
NOP generator active
U12 Disconnects RAM DB
when
NOP generator active

Keyboard Interface (U15)
40 key (10 colums, 5 row) orgaized as
two sets of 20 key (5 x 4)

Cassette Interface signal fixer
Uses CPU's /SO pin as single bit input and
/OUT memory acces to create audio

Cassette input

Cassette output

Sync Generation (U6/7, U10A/B, U6A, U4F)
16-bit counter using 2MHz Clock.

HSYNC – for each line,
From 60-63uS for 4uS,
MOD-64, S Count 0bxxxxxxxxxx1111yyy

ROW – 3-bit Character row counter
MOD-8, S count 0bxxxxxRRRxxxxxxx

VSYNC – line 292 for 4 lines,
total 256uS,
S Count 0b1001001yyxxxxxxx

NMI – line 312, Assert NMI. Reset Counters
S count 0b100111000xxxxxxx,

JITTER – 8-bit counter (U11)
Clocks since last reset/NMI Asserted
MOD-256, S count 0bxxxxxxxxJJJJJJJJ

PSU
Vanilla 9V to 5V Linear voltage regulator

MX-78 – A 6502 Powered Tiny Basic Personal Computer with PAL TV interface

Sheet: /	V.Crabtree	
File: MX78PoC.kicad_sch		
Title:		
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