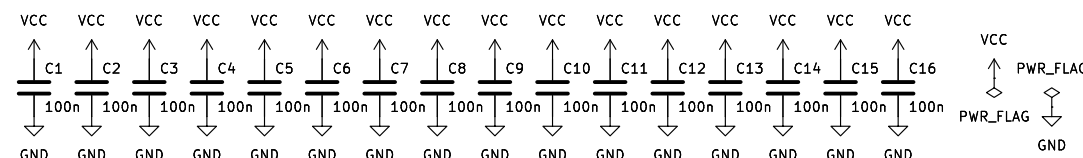
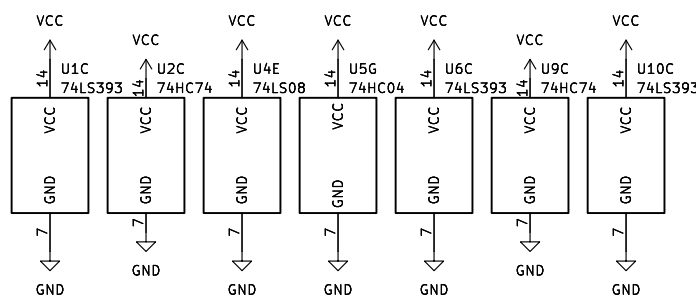
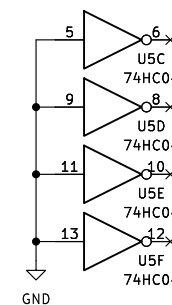
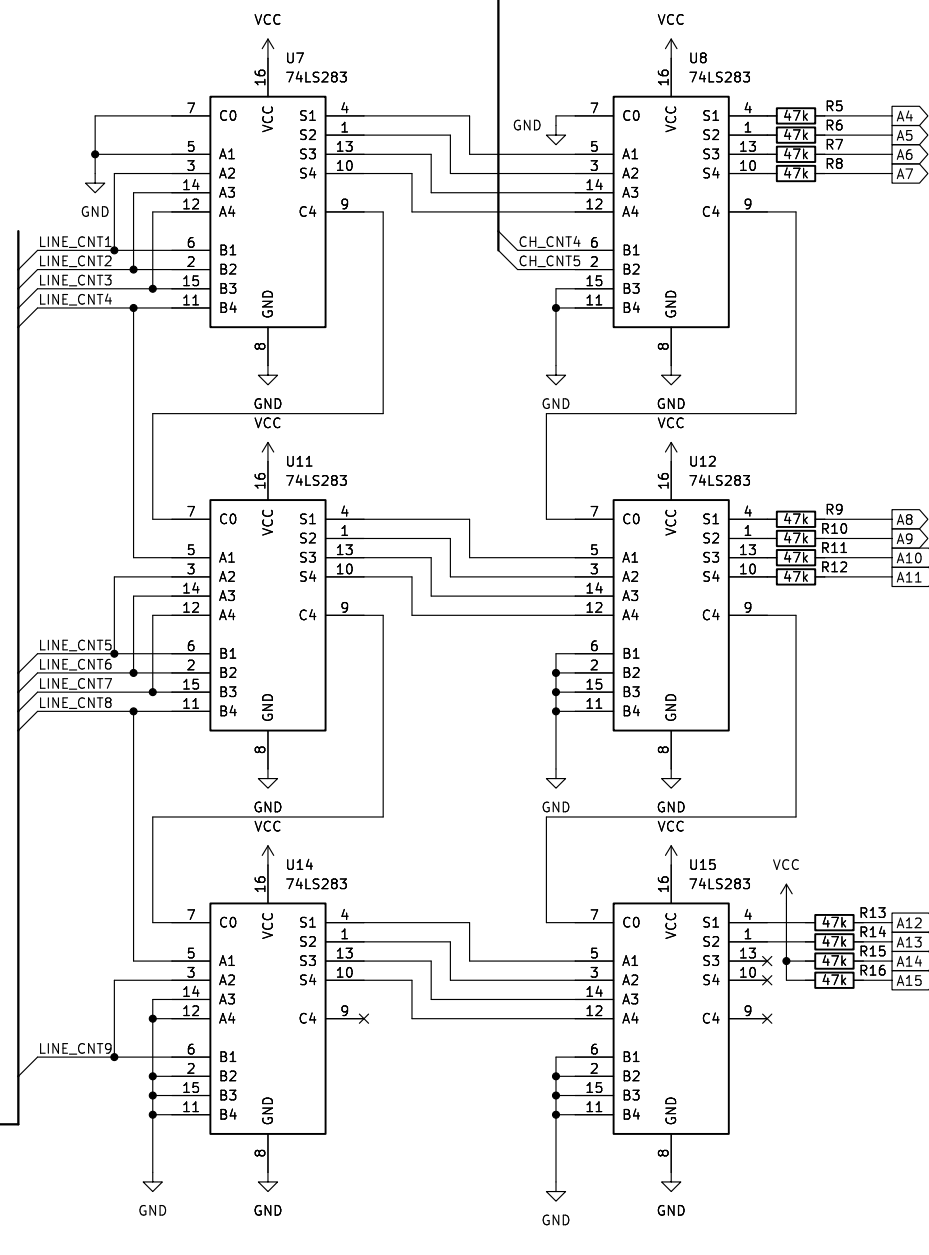
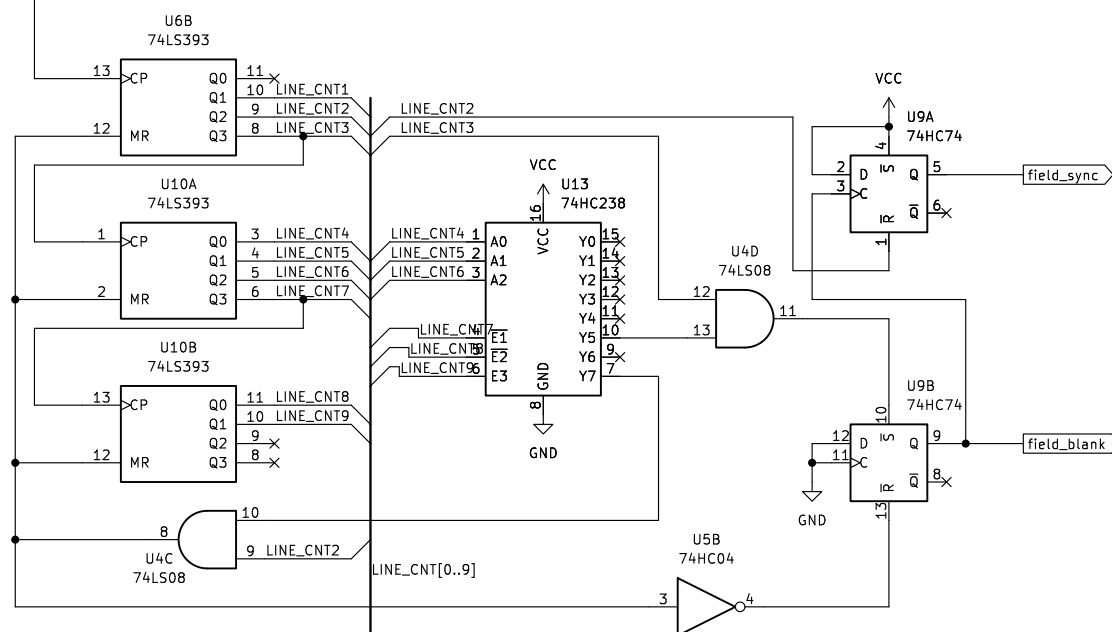


Address generation:
 $\text{Line count} \times 0x30 + \text{character count}$
 (each line twice)



pixel addressable 384x300 video at 20MHz dot clock

DNB projects

Sheet: /Line timing/
 File: line_timing_sch.kicad_sch

Title: SVGA address and sync timing generator

Size: A3 Date: 2023-11-16
 KiCad E.D.A. kicad 7.0.9

Rev: a
 Id: 2/2