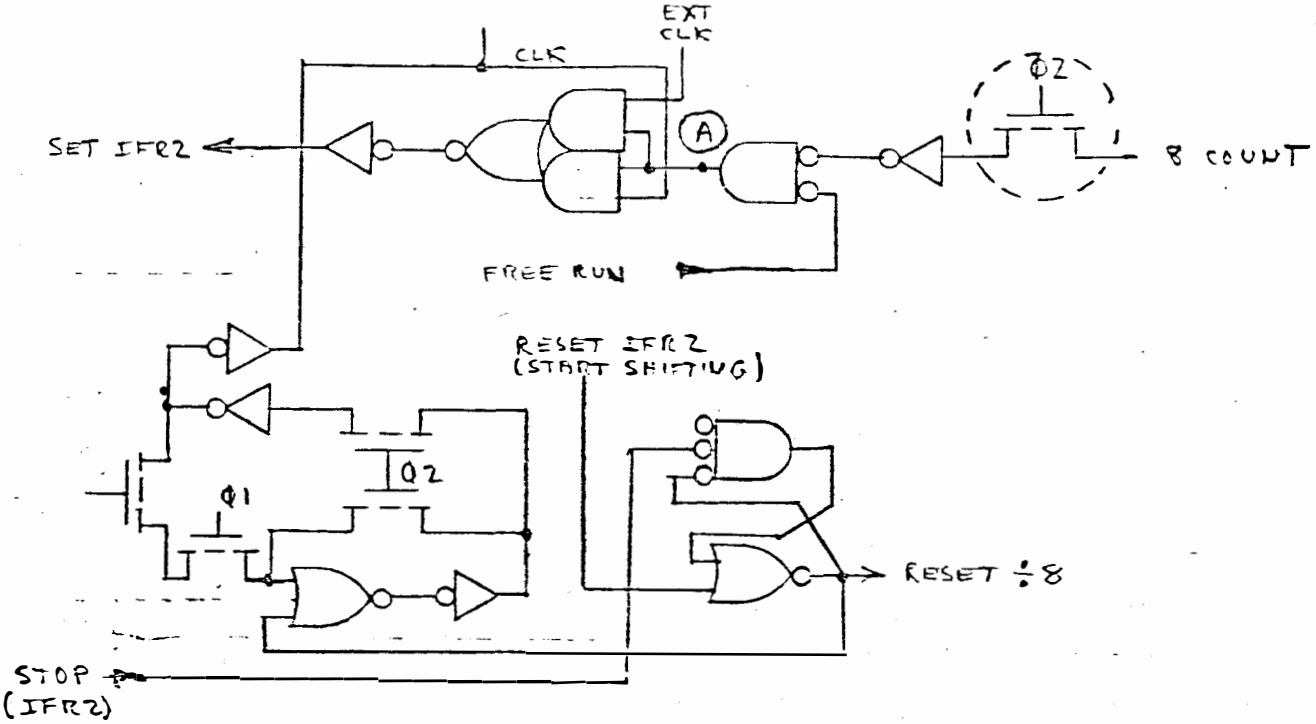
NEVER MADE

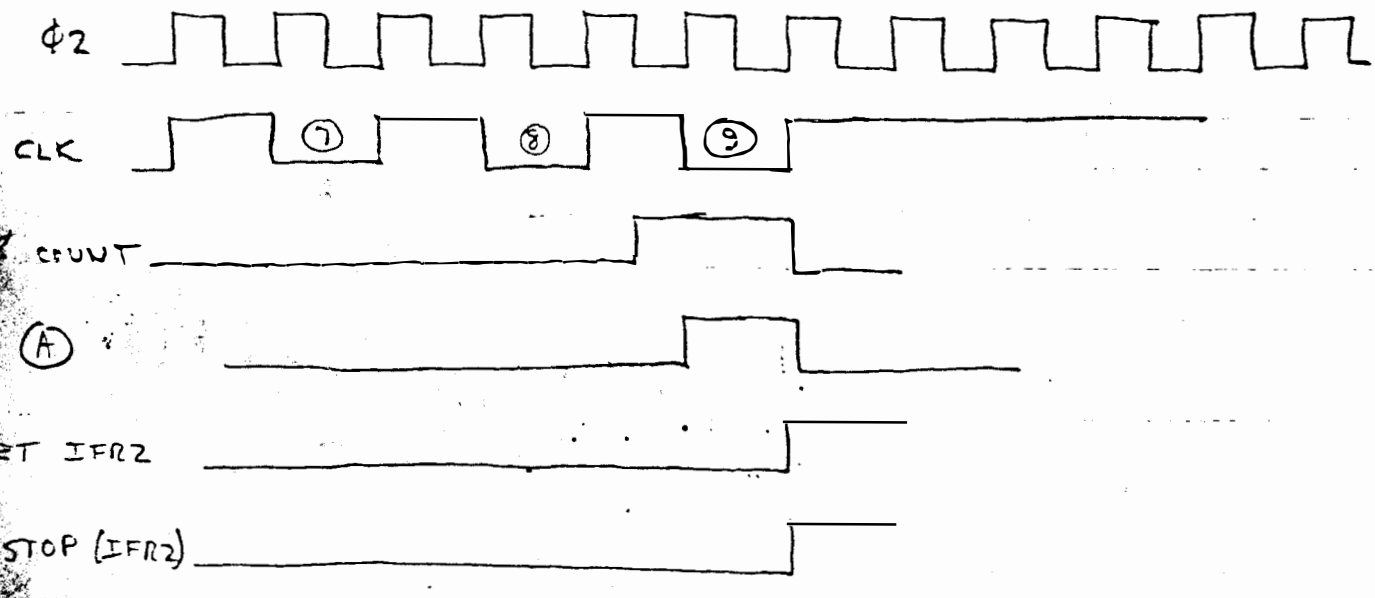
MCS 6522 PROBLEMS AND PROPOSED CORRECTIONS

R. Gop 9/

① PROBLEM: NINE CLOCK PULSES ARE OUTPUTTED WHEN SHIFTING IN AT THE SYSTEM CLOCK RATE. HOWEVER, THIS IS NOT THE CASE WHEN SHIFTING OUT.

CORRECTION: THE LOGIC CAUSING THIS PROBLEM IS AS BELOW:

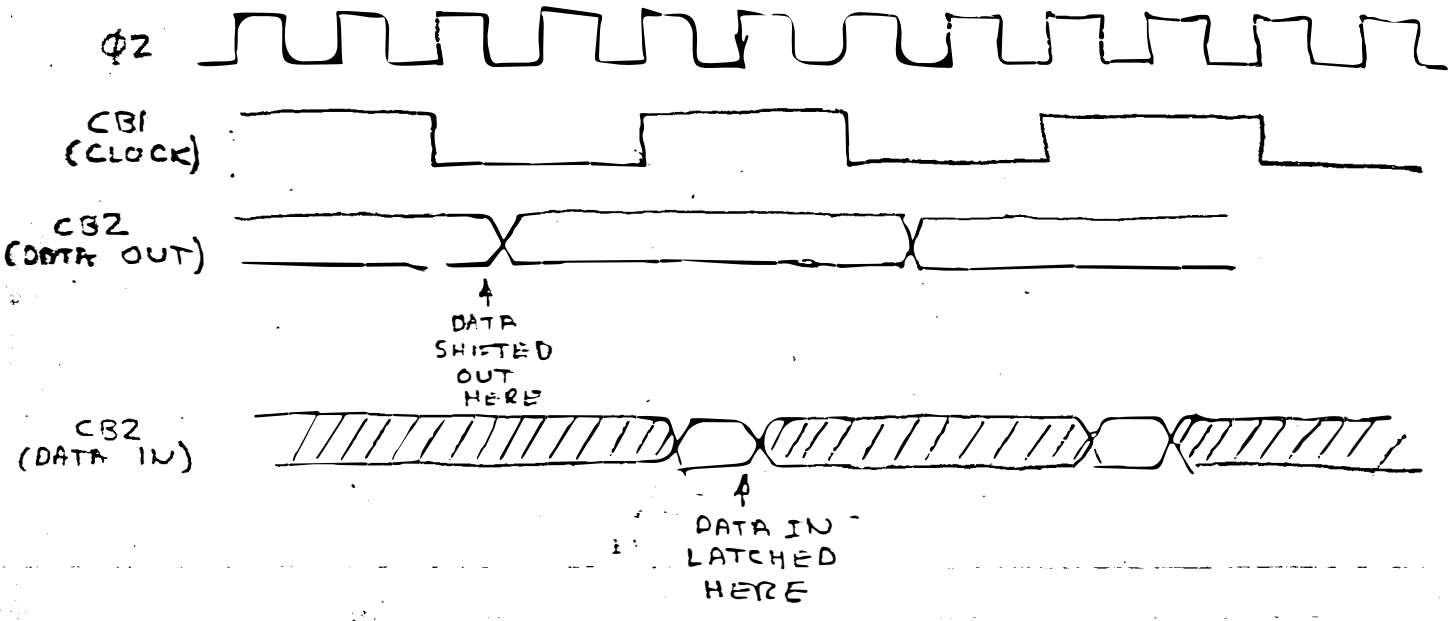




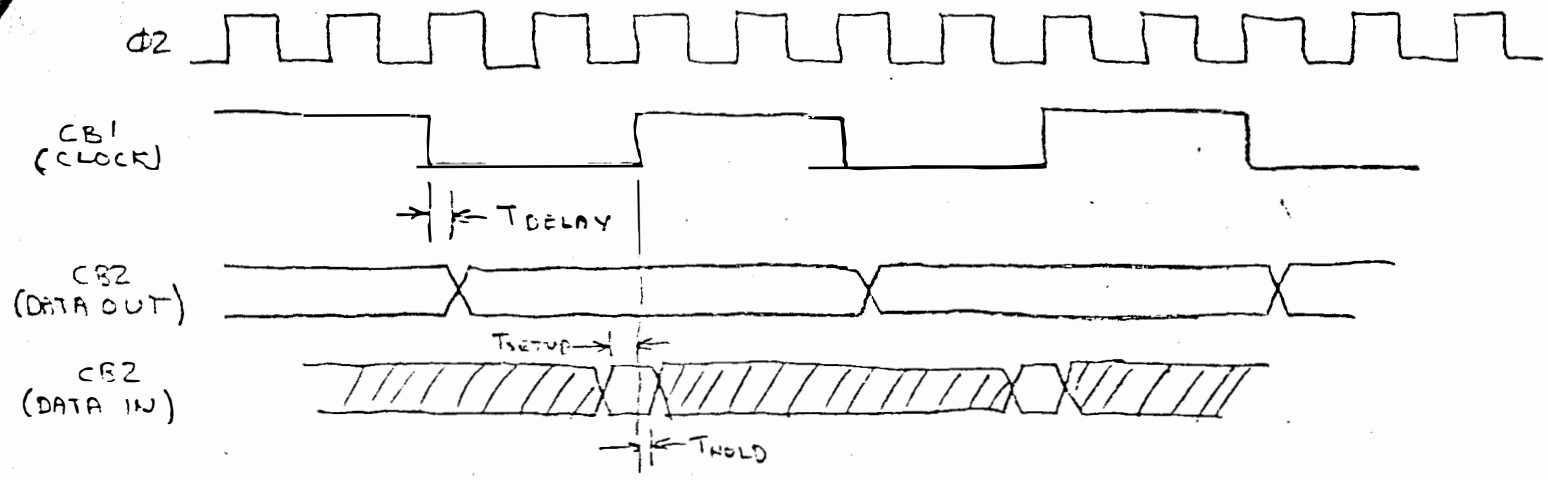
IT CAN BE SEEN FROM THE TIMING DIAGRAM THAT THE SHIFT CLOCK STOP COMES AFTER THE NINTH CLOCK PULSE HAS ALREADY BEEN SHIFTED OUT. BY ELIMINATING THE CIRCLED PASS TRANSISTOR, THE IFR2 BIT WILL BE SET 1½ CYCLES EARLIER, THEREBY PREVENTING THE NINTH CLOCK PULSE FROM BEING GENERATED.

(2) PROBLEM: DATA SHIFTED IN OR OUT IS NOT REFERENCED TO THE CB1 CLOCK EDGE

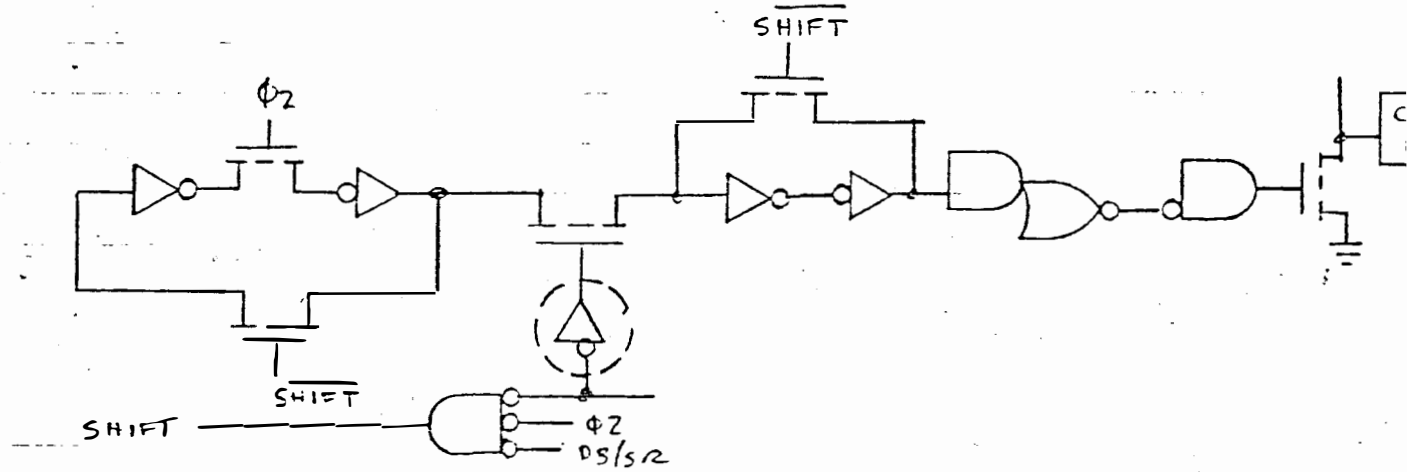
CORRECTION! PRESENTLY THE TIMING OF THE DATA SHIFTED IN OR OUT IS AS REPRESENTED BELOW

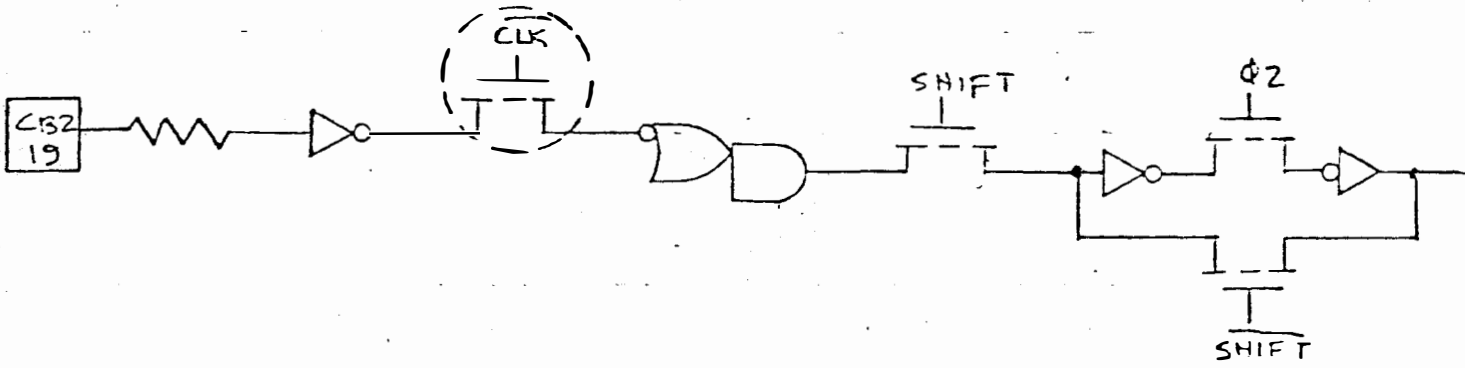


THE TIMING SHOULD BE MODIFIED SO THAT DATA IS REFERENCED TO THE CLOCK EDGE AS SHOWN BELOW!



THE OUTPUT AND INPUT CHANGES TO IMPLEMENT THIS TIMING ARE SHOWN CIRCLED BELOW





③ PROBLEM: WHEN SHIFTING IN OR OUT UNDER CONTROL OF T2, THE TIME FROM A SR READ OR WRITE TO THE FALLING EDGE OF THE FIRST CLOCK PULSE DEPENDS UPON THE INITIAL CONTEN OF T2.

CORRECTION: T2 SHOULD BE INITIALIZED WITH A T2L-L TO T2C-L TRANSFER PRIOR TO THE START OF THE SHIFTING OPERATION, (SEE SCHEMA

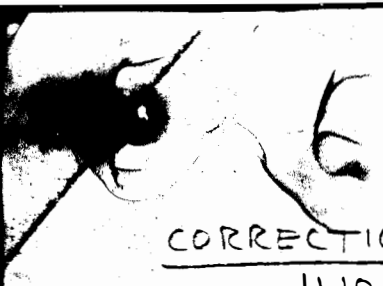
④ PROBLEM: A SR READ WILL INITIATE A SHIFT OUT OPERATION DURING A SHIFT OUT MODE AND A SR WRITE WILL INITIATE A SHIFT IN OPERATION DURING A SHIFT IN MODE. THESE ARE UNREALISTIC CONDITIONS.

CORRECTION: A SHIFT OUT SHOULD ONLY BE INITIATED BY A SR WRITE AND A SHIFT IN SHOULD ONLY BE INITIATED BY A SR READ, (SEE SCHEMAT

⑤ PROBLEM: THE 6522 SHIFTS IN OR OUT THE MSB FIRST WHICH IS CONTRARY TO NORMAL PRACTIC

CORRECTION: EITHER LEAVE AS IS AND CHANGE ON FUTURE 6523, OR CHANGE LOGIC TO SHIFT IN OR OUT LSB FIRST.

⑥ PROBLEM: DURING A SHIFT OUT USING SYSTEM CLOC OPERATION, THE TIME FROM THE SR WRITE TO THE FALLING EDGE OF THE FIRST CLOC PULSE IS EITHER 1½ OR 2½ Φ2 CYCLES DEPENDING UPON WHETHER THE IFR2 BIT IS CLEARED OR SET AT THE TIME.



CORRECTION: THE FIRST CLOCK EDGE SHOULD BE INDEPENDENT OF THE STATE OF IFR2. THIS EDGE WILL COME 1 1/2 CYCLES AFTER THE SR WRITE WITH THE LOGIC CHANGE SHOWN IN THE SCHEMATIC.

(7) PROBLEM: A SHIFT REGISTER EXTERNAL CLOCK INPUT CAN NOT BE COMPLETELY ASYNCHRONOUS WITH THE $\phi 2$ CLOCK. IF THE EXTERNAL CLOCK EDGE OCCURS WITHIN ABOUT 50 nS BEFORE THE FALLING EDGE OF $\phi 2$, IT IS POSSIBLE FOR THE SHIFT REGISTER AND BIT COUNTER TO IGNORE THE TRANSITION

CORRECTION: EITHER CHANGE SPEC. TO REFLECT ACTUAL REQUIRED TIMING OF INPUT OR PREFERABLY CORRECT LOGIC AND MAKE INPUT COMPLETELY ASYNCHRONOUS BY MODIFING LOGI AS SHOWN ON SCHEMATIC.

(8) PROBLEM: THE TRANSISTOR APPARENTLY USED FOR TRANSFERS FROM THE DATA BUS TO THE INTERRUPT FLAG REGISTER IS TOO SMALL FOR THAT PURPOSE. THIS FUNCTION IS NOT COVERED IN THE SPEC, ALTHOUGH IT PROBABLY WOULD BE VERY USEFUL TO INDIVIDUALLY CLEAR INTERRUPT FLAG BITS.

CORRECTION: REPLACE TRANSISTOR ON S-R FLOP OUTPUT WITH ANOTHER INPUT TO FLOP (SEE SCHEMATI