HITACHI
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Hard Disk Drive Specifications

Hitachi Microdrive®

Models

8GB	3K8-8
6GB	3K8-6
4GB	3K8-4

Revision 2.10 **26.May.2006**

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EC History

Rev.1.00	14 Nov. 2005	Initial Release
Rev.1.01	5 Dec, 2005	modify
Rev.2.00	31 Mar. 2006	Extra Sensory Protection (E.S.P.) support model
Rev.2.01	7 Apr, 2006	correction
Rev.2.02	20 Apr, 2006	Added description of Format Unit command
Rev.2.10	26 May, 2006	Correction on set E.S.P sensitivity command, total bytes

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1 General

This document describes the characteristics of 1.0” type 3600 RPM Hard Disk Drive with capacities of 8GB, 6GB and 4GB. This drive is the Hitachi Global Storage Technologies Microdrive® and is hereafter referred to as “the drive” or “the device”. This document defines the hardware functional and interface specifications. The drive is available in the following models:

8GB 3K8-8	HMS361008M5CE00
6GB 3K8-6	HMS361006M5CE00
4GB 3K8-4	HMS361004M5CE00

1.1 Reference

Information Technology-AT Attachment with Packet Interface-4
Information Technology-AT Attachment with Packet Interface-7

1.2 Abbreviations

Kbits	1,000 bits
Mbps	1,000,000 bits per second
KB	1,024 bytes
MB	1,000,000 bytes
GB	1,000,000,000 bytes
Kbit/mm	1,000 bits per millimeter
Mb/sq-mm	1,000,000 bits per square millimeter
drive	3K8-8, 3K8-6, 3K8-4
device	3K8-8, 3K8-6, 3K8-4
TBD	to be defined

1.3 Drive handling precautions

The drive can be easily damaged by shock or Electric Static Discharge (ESD). Any damage incurred by the drive after removal of it from the shipping package and opening of the ESD protective bag is the user's responsibility.

Do not apply pressing force onto the top or bottom surface of the drive.

DO NOT PRESS!

DO NOT PRESS WHEN REMOVING THE DRIVE

DO NOT PRESS WHEN CARRYING THE DRIVE

DO NOT APPLY PRESSURE WHEN ATTACHING THE DRIVE

Do not steal the breather hole on the top cover.

DO NOT SEAL THIS HOLE!

SEALING THIS HOLE WILL RESULT IN LOSS OF DATA

1.4 General Features

- 8GB, 6GB and 4GB formatted capacity
- 512bytes/sector
- Integrated controller
- Multi Zone recording
- No-ID recording format
- ME2PR 60/62 coding
- Enhanced ECC On-The-Fly
- 42.5 bytes Read Solomon Code
- 20 bytes On-The-Fly correction
- 128KB cache (total buffer 384KB, upper 256KB is used for firmware)
- Fast data transfer rate
- Up to 16.7MB/sec at PIO mode 4
- Up to 16.7MB/sec at Multiword DMA mode 2
- Up to 33.3MB/sec at Ultra DMA mode 2
- Media data transfer rate 126Mbits/sec (8GB outer , typical) – 68 (8GB inner, typical)
- Closed loop actuator servo (Embedded Sector Servo)
- True Track Servo
- Rotary voice coil motor actuator
- Load/Unload mechanism
- Mechanical latch
- Adaptive power save control
- 1.2sec Power on standby state to ready
- Extra Sensory Protection (E.S.P.) for free drop detection/protection (Optional feature)
- Shock resistance
  - Non-operation : 19600 m/sec^2 / 1ms (2000G/1ms)
  - Operation : 3920 m/sec^2 / 2ms (400G/2ms)
  - Operation : 19600 m/sec^2 / 1ms (2000G/1ms) with E.S.P. Option

Part 1. Functional Specifications

2 Fixed disk subsystem description

2.1 Control Electronics

The control electronics works with the following function:

Embedded Sector Servo

No-ID™ format

Multi zone recording

ME2PR 60/62 Code

ECC On-The-Fly

Extra Sensory Protection™(E.S.P.) (Optional)

Enhanced Adaptive Battery Life Extender (ABLE-3)

2.2 Head Disk Assembly

The following technologies are used in the drive:

Femto slider

Smooth glass disk

GMR head

Integrated Lead suspension (ILS)

Load/Unload mechanism

Mechanical latch

3 Fixed Disk Characteristics

3.1 Formatted Capacity

The logical drive parameters in Identify Device data are as follows:

Description	3K8-8	3K8-6	3K8-4
Bytes per Sector	512	512	512
Sectors per track	201-345	192-312	144-264
Number of Heads	2	2	2
Number of Disks	1	1	1
RPM	3600	3600	3600
Number of Heads	16	16	16
Sectors per Track	63	63	63
Number of Cylinders	15,501	11,905	7,936
Number of Sectors	15,625,008	12,000,556	799,488
Total Logical Data Bytes	8,000,004,096	6,144,284,672	4,095,737,856

Table 1 Formatted Capacity

3.2 Data Sheet

Rotational Speed (RPM)	3600
Data Transfer rates (buffer to/from media)(typical)	68 – 126 Mbps
Data Transfer rates (host to/from buffer)	16.7 MB/sec (PIO Mode 4) 16.7 MB/sec (Multiword DMA mode 2) 33.3 MB/sec (Ultra DMA mode 2)
Recording Density (kBPI)	850 (Maximum)
Track Density (kTPI)	126 (Maximum)
Areal Density (Gbit/sq-in)	94.4 (Maximum)
Data Bands	24

Table 2 Data Sheet

3.3 Performance Characteristics

Drive performance is determined by the following parameters:

Command overhead

Mechanical positioning

Seek time

Latency

Data transfer speed

Buffering operation (Read ahead/Write cache)

Note: All the above parameters contribute to drive performance. Other parameters also contribute to the performance of the actual system. This specification describes only the characteristics of the drive, not the system throughput which depends on the system and the application.

The following table gives typical value of each parameter. Detailed descriptions follow in the next sections.

	Typical
Average random seek time of read	12 (msec)
Average random seek time for write	13 (msec)
Rotational speed	3600 (RPM)
Power on standby to ready	1 (sec)
Command overhead	1 (msec)
Disk-buffer data transfer rate	68 – 126 (Mbps)
Buffer-host data transfer rate	33 (MB/sec) (*1)

Note *1) Ultra DMA mode 2

Table 3 Performance parameters

3.3.1 Command Overhead

Command overhead is defined as the total time from the receipt of the command by the drive to start of motion of the actuator.

3.3.2 Mechanical positioning

Average Seek Time (Including Settling)

Command Type	Typical (msec)	Max (msec)
Read	12	14
Write	13	15

Table 4 Mechanical positioning performance

Headings “Typical” and “Max” are given throughout the performance specification. “Typical” means the average of the drive population tested at nominal environmental and voltage conditions. “Max” means the maximum value measured on any drive over the full range of environmental conditions. The seek time is period of time from the start of the motion of the actuator to the start of reliable read or write operation. A reliable read or write implies that error correction/recovery is not employed to correct arrival problems. The average seek time is a measure of the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{max}(max+1-n)(Tn_{in} - Tn_{out})}{(max+1)(max)}$$

Where:

n = Seek Length (1 to max)

Tn_{in}= Inward measured seek time for an n track seek

Tn_{out}= Outward measured seek time for an n track seek

Full Stroke Seek Time

Command Type	Typical (msec)	Max (msec)
Read	24	27
Write	24	27

Full stroke seek is measured as the average of 1000 full stoke seeks.

Table 5 Full stroke seek time

Single Track Seek Time

Command Type	Typical (msec)	Max (msec)
Read	2.0	3.0
Write	3.0	4.0

Note: Single track seek time does not include command overhead but include settling.
Single track seek time is an average. The single track seek time is calculated by adding the time of inward and outward seek time of each single track and dividing that sum by the total number of tracks.

Table 6 Single track seek time

Average Latency

Rotational Speed(RPM)	Time for a revolution(ms)	Average Latency(ms)
3600	16.7	8.3

Table 7 Latency Time

Drive Ready Time

Condition	Typical(sec)	Max(sec)
Power on to interface ready	0.1	0.1
Power on standby to Idle	1.2	1.4
Standby to Idle	0.5	0.6

Note: The drive powers up in Standby mode as default. Drive ready time is defined as:

- Power on to interface ready
- Standby state right after the power on to Idle
- Standby state to Idle

Table 8 Drive Ready Time

Operating modes

Operating Mode	Description
Spin-Up	Start up time period from spindle stop.
Seek	Seek operation mode.
Write	Write operation mode.
Read	Read operation mode.
Performance Idle	The drive is capable of responding immediately to media access requests. All electronic components remain powered and full frequency servo remains optional.
Active Idle	The drive is capable of responding immediately to media access requests. Some circuitry including servo system and R/W electronics is in power saving mode. The head is parked near the mid-diameter of the disk with open looped control.
Low Power Idle	Spindle motor is rotating normally with actuator unloaded. The drive interface is capable of accepting commands.
Standby	Spindle motor is stopped. All circuitry except the host interface is in low power saving mode. The execution of commands is delayed until spindle motor becomes ready.
Sleep	Same as Standby

Table 9 Operating modes

Operating mode at power on

The drive powers up in Standby mode as default.

Adaptive Power Save Control

The transition timing from Performance Idle to Standby depends on both the access pattern of the host system and the setting of the advanced power management level. With the power-on default, the transition timing for each power mode is under control of Adaptive Battery Life Extender algorithm.

4 Data Integrity

4.1 Data loss at power off

Power off during any operations except for write operation will not cause any data loss.
Power off during a write operation causes the loss of data received by the drive but not yet written onto the disk media.
There is a possibility that power off during a write operation might make (a) sector(s) of data unreadable. This state can be recovered by a rewrite operation.

4.2 Write Cache

When write cache is enabled, there is a possibility that the write command completes before the actual disk write operation finishes. This means that there is a possibility that a power off event may occur even after a full write command finishes. This means that it is possible that even after a write command completion a power off might cause the loss of the data which the drive has received but not yet written onto the disk.
In order to prevent data loss, confirm the completion of the actual write operation prior to the power off by issuing the Flush Cache, Standby Immediate or Sleep command and confirming its completion.
The default state of the write cache at power-on is “Disabled”.

4.3 Write Safety

The drive ensures that the data is written onto the disk media properly. The following conditions are monitored during a write operation. When one of those conditions exceeds the criteria, the write operation is terminated and automatic retry sequence will be invoked.
Head off track
External shock
Low supply voltage
Spindle speed tolerance
Head open/short

4.4 Data Buffer Test

The data buffer is tested at Power-on-reset. The test consists of a write/read “00”x and “ff”x pattern on each buffer position.

4.5 Error Recovery

Errors occurring on the drive are handled by the Error Recovery Procedure (ERP). Errors that are uncorrectable after application of the error recovery procedure are reported to the host system as non-recoverable errors.

4.6 Automatic Reallocation

The sectors those show some errors may be reallocated automatically when specific conditions are met. The drive does not report automatic reallocation to the host system. The conditions for automatic reallocation are described below.

4.6.1 Non-recovered Write Errors

When a write operation can not be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error reported to the host system only when the write cache is disabled and the auto reallocation has failed.

4.6.2 Non-recovered Read Errors

When a read operation has failed after defined ERP is fully carried out, a non-recovered error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, the sector is reallocated.

4.6.3 Recovered Read Errors

When a read operation for a sector fails once and is then recovered at the specific ERP steps, the sector is reallocated automatically. A media verification sequence may be run prior to the reallocation according to the predefined conditions.

5 Zone Format

The following table shows zone format of typical 8GB drives.

Zone	Cylinder	Sector per track
0	0 – 1279	345
1	1280 – 2559	345
2	2560 – 3711	345
3	3712 – 4863	345
4	4864 – 5887	345
5	5888 – 6783	336
6	6784 – 7679	336
7	7680 – 8575	336
8	8576 – 9471	324
9	9472 – 10495	324
10	10496 – 11519	316
11	11520 – 12543	312
12	12544 – 13695	288
13	13696 – 14847	288
14	14848 – 15871	288
15	15872 – 17151	270
16	17152 – 18431	264
17	18432 – 19839	252
18	19840 – 21247	252
19	21248 – 22655	240
20	22656 – 23935	230
21	23936 – 25087	230
22	25088 – 26239	205
23	26240 -	201

Table 10 Zone format

6 Specification

6.1 Environment

6.1.1 Temperature and humidity

Operating conditions	
Temperature	5 – 60 ˚C (Note 1)
Relative humidity	8 – 90 %, non condensing
Maximum wet bulb temperature	29.4 ˚C, non condensing
Maximum temperature gradient	20 ˚C / Hour
Altitude	-300 to 3048 m
Non operating conditions	
Temperature	-40 – 70 ˚C
Relative humidity	5 – 95 %, non condensing
Maximum wet bulb temperature	40 ˚C, non condensing
Maximum temperature gradient	20 ˚C / Hour
Altitude	-300 to 12,192m

Note 1: Regardless of the ambient temperature, the drive can be operated at a maximum temperature of 60 ˚C at center of the base spindle motor of the drive.

Note 2: Maximum storage period with shipping package is one year.

Table 11 Temperature and humidity specifications

Corrosion Test

The drive is functional and does not show no signs of corrosion after being subjected to temperatures of 50 ˚C with 90% relative humidity for one week of storage followed by a return to 25 ˚C with 40% relative humidity in two hours.

6.1.2 Radiation noise

The drive works without degradation of the soft error rate under the following magnetic flux density limit at the enclosure surface.

Frequency	Limits (uT RMS)
0 – 60	500
61 – 100	250
101 - 200	100
201 - 400	50

Table 12 Radiation noise

6.1.3 Conductive noise

The drive works without degradation of the soft error rate with an AC current of up to 45mA(p-p) in the frequency rage from DC to 20MHz via a 50 Ohm resister.

6.1.4 Magnetic Fields

The drive withstands the radiation and conductive noise limits shown above.

6.2 DC Power Requirements

Connection to the drive should be made in safety extra low voltage (SELV) circuit.

Power supply		
Nominal supply	+3.3 Volts	5
Power supply ripple	70mV p-p max	1
Tolerance	+5/-15%	2
Supply Current (nominal condition, population mean)		
Performance Idle	150 (mA)	
Active Idle	95 (mA)	
Low Power Idle	80 (mA)	
Read	190 (mA)	3
Write	190 (mA)	3
Seek	160 (mA)	
Standby	20 (mA)	
Peak	310 (mA)	4

Notes:

1. The maximum fixed disk ripples is measured at 3.3V input of the drive.
2. The drive will not be incurred damage for an over voltage condition of +25% (maximum duration of 20 (msec)) on the 3.3V.
3. The read/write current is specified as RMS of 200 msec.
4. The worst case operating current at unloading
5. Power line capacitance 120uF max. Power on rising time(10% - 90%) 0.1msec.(min.), 3.0msec.(max.) are required.

6.3 Reliability

6.3.1 Load/Unload Cycles

The drive will meet the specified error rates after the following Load/Unload cycles:

- 300,000 cycles (Load/Unload to be controlled by the drive firmware)
- 20,000 cycles (Load/Unload are not controlled by the drive firmware)

6.3.2 Warranty

The warranty will be covered by the contracts.

6.3.3 Life

To be discussed separately.

6.3.4 Preventive Maintenance

None required.

6.4 Error Rates

Error rates fall into two categories:

- Recoverable errors
- Non-recoverable errors

The following error rates assume that no attempts are made to read or write in areas already identified as being defective. The error rates are defined for the drive operating at the full range of environmental conditions and are shown in 6.1 Environment. The voltage limits are shown in 6.2 DC Power Requirements.

6.4.1 Recoverable Errors

A recoverable error is defined as an operation that failed the first time but succeeded in recovering the error when the drive error recovery procedure was invoked. ECC On-The-Fly, which is always active, is transparent to the system and is not counted as a recoverable error.

A typical drive shall have no more than one recoverable error per 100 million bits transferred (1 in 10^8) when operated at nominal voltage and environment condition. The typical disk drive error rate represents the geometric mean of the error rates of the total disk drive population. The size of the drive population should be 50 drives or more.

Each drive in the population shall have no more than one recoverable error per 10 million bits transferred (1 in 10^7) when operated at full range of voltage and environment conditions and the operating vibration levels stated in 6.6 Vibration and Shock.

6.4.2 Non-recoverable Errors

A non-recoverable error is defined as an operation that failed and was not recovered by the drive error recovery procedure. No drive has more than one non-recoverable error per 10 trillion bits transferred (1 in 10^{13}) when operated at the full range of voltage and environmental conditions.

6.5 Mechanical Specifications

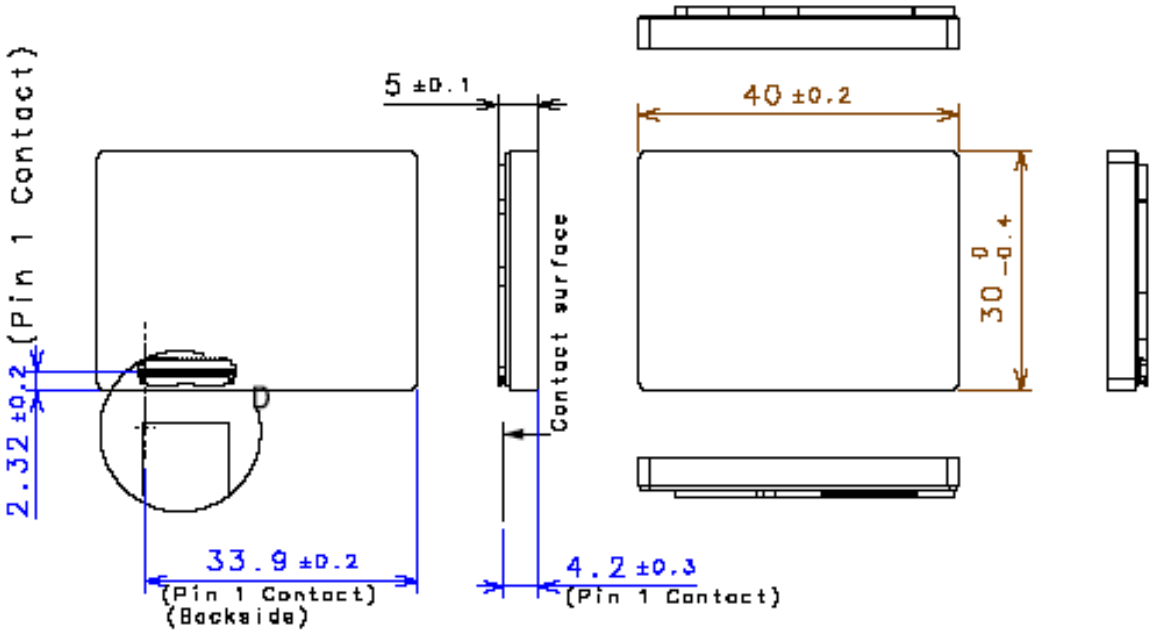
6.5.1 Physical dimensions and weight

The following table lists the dimensions and weight of the drive.

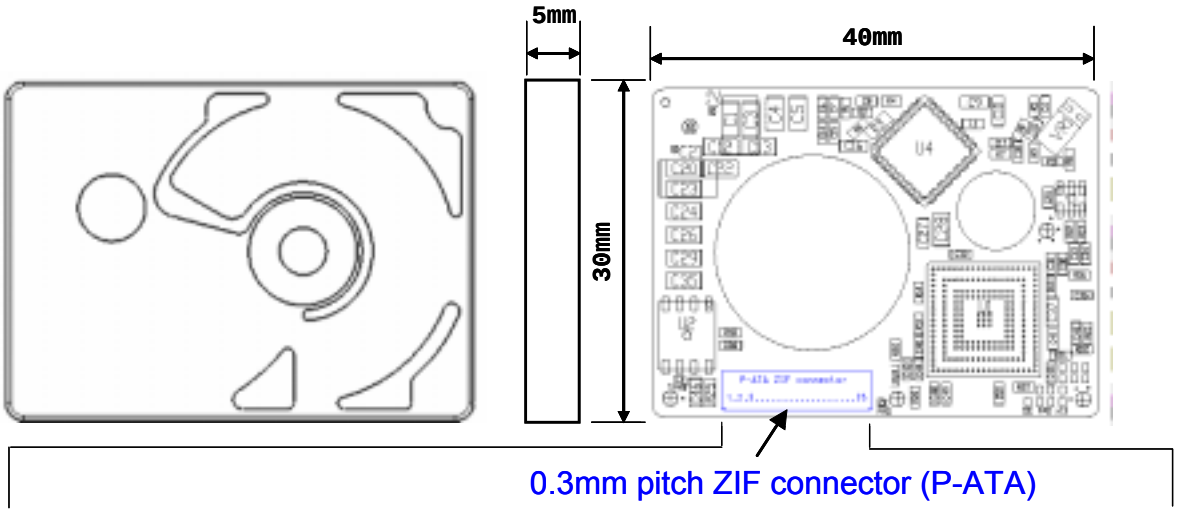
Height (mm)	5.0±0.1
Width (mm)	40±0.2
Length (mm)	30+0/-0.4
Weight (grams)	13 (typcial)

Table 13 Physical dimensions and weight

6.5.2 Mechanical dimensions



6.5.3 Connector



Pin	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
	GND	DD10	DD09	DD02	DD08	DD01	PDIAG-	DD00	DASP-	DA00	DMACK-	DA01	DMARQ	DA02	IORDY	RESET-	CSEL-	VCC	VCC	INTRQ	DIOW-	DIOR-	CS1-	CS0-	DD15	DD07	DD14	DD06	DD13	DD05	DD12	DD04	DD11	DD03	GND

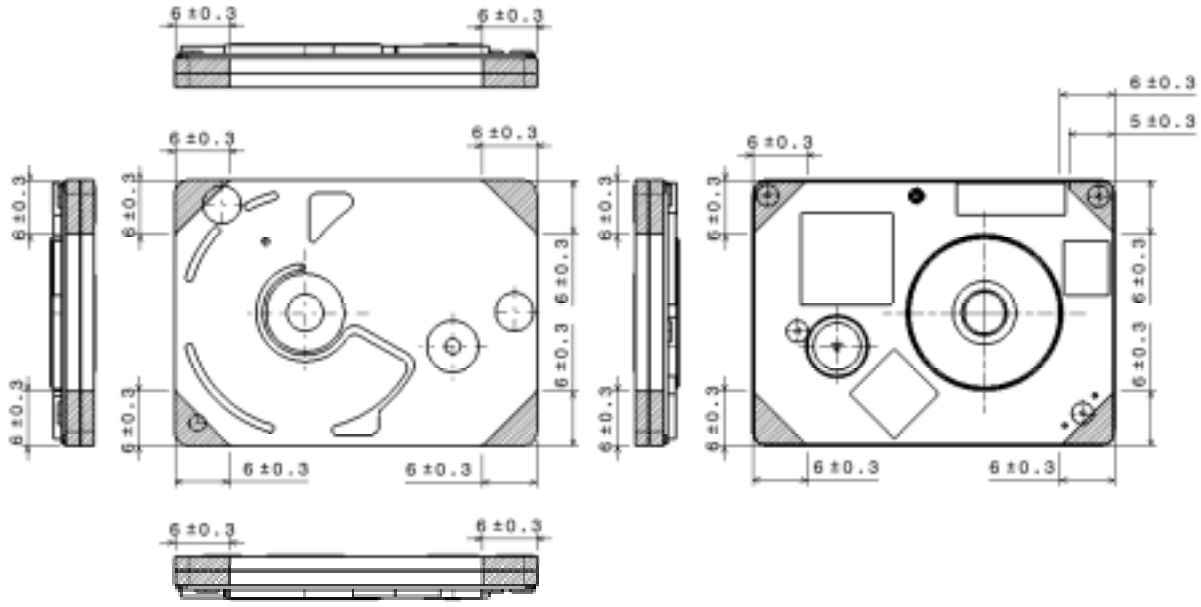
6.5.4 Mounting orientation

The drive will operate in all axes (360 ˚).

Performance and error rate will stay within specification limits if the drive is operated in the other permissible orientations from which it was formatted. Thus a drive formatted in a horizontal orientation is able to run vertical and vice versa. Vibration test and shock test are to be conducted by mounting the drive to the test table using special fixture.

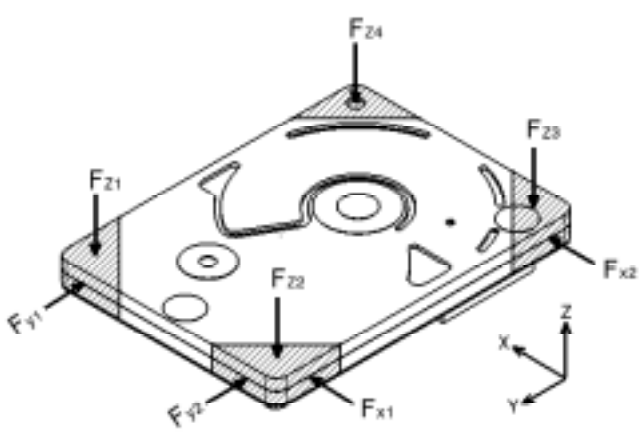
Mounting Considerations

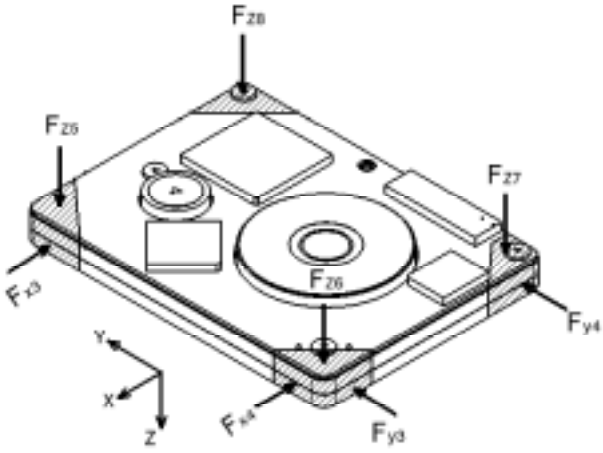
Mounting area (hatched area) is defined as below. This area was used to fix the drive to the equipment.



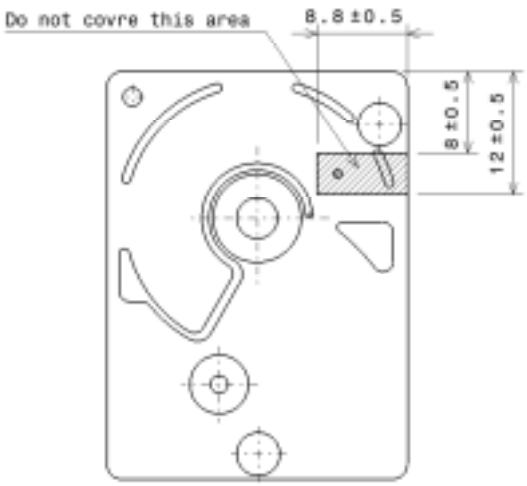
Mounting force is 7.4N MAX at each area.

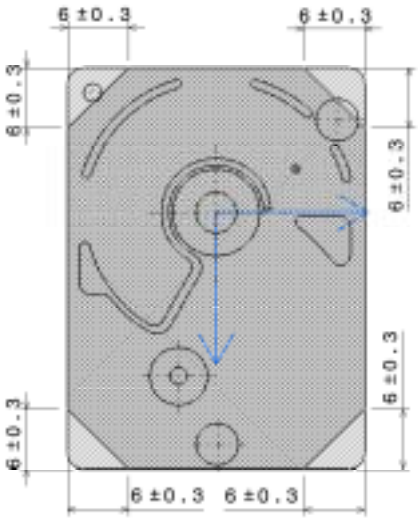
After mounting there is no twist and bending force act the device.





Breather Hole





Cover Stiffness

External force

At cross hatched area

0.156 N/mm^2

Total 2N MAX

6.5.5 Load/Unload Mechanism

The head load/unload mechanism is provided to protect the disk during shipping, movement, or storage. Upon power down, a head unload mechanism secures the heads at the unload position.

6.6 Vibration and Shock

All vibration and shock measurements in this section are for the drive without the mounting material for the system.

6.6.1 Operating vibration

Operating random vibration

The test consists of 30 minutes of random vibration using the power spectral density (PSD) levels specified in C-S 1-9711-002 (1990-03) as V5L. The vibration test level for V5L is 6.57 m/sec^2 RMS.

Frequency	(m/sec^2)^2
5	1.92xE-3
17	1.05xE-1
45	1.05xE-1
48	7.68xE-1
62	7.68xE-1
65	0.96xE-1
150	0.96xE-1
200	4.80xE-2
500	4.80xE-2

Table 14 Random vibration

Operating swept sine vibration

- 9.8 m/sec2 (Zero-to-peak), 5 to 500 to 5Hz sine wave
- 2.0 oct/min sweep rate

6.6.2 Non-operating vibration

Non-operating random vibration

The test consists of a random vibration applied in each of three mutually perpendicular axes with 15 minutes duration per axes. The Power Spectral Density (PSD) level for the test simulates the shipping and relocation environment which is shown below.

Frequency (Hz)	Power Spectral Density ($(m/sec^2)^2/Hz$)
2.5	0.096
5	2.88
40	1.728
500	1.728

Note: Overall RMS level of vibration is 29.49 m/sec^2 RMS.

Table 15 Random vibration PSD profile breakpoints (non-operating)

Non-operating swept sine vibration

- 49 m/sec^2 (zero-to-peak), 10 to 500 to 10 Hz sine wave
- 0.5 oct/min sweep rate

6.6.3 Operating Shock

The drive meets the following criteria while operating under the conditions described as follows:

- The shock test consists of ten shock inputs in each axis and direction for a total of 60 shocks.
- There must be a minimum delay of 3 seconds between shock pulses. Recoverable errors and automatic retries are allowed during the test.
- No data loss or permanent damage occurs during a half-sine shock pulse of 3920 m/sec^2 of 2 msec duration and a half-sine shock pulse of 98 m/sec^2 of 11 msec duration.

6.6.4 Non-operating shock

The drive withstands with no damage a half-sine wave shock pulse of 1176 m/sec^2 of 11 msec duration and a half-sine wave shock pulse of 19600 m/sec^2 of 1 msec duration on six sides when the heads are unloaded. (When the power is not applied to the drive, the heads are automatically located on the unloaded position.)

All shocks shall be applied in each direction of the drive's three mutually perpendicular axes, one axis at a time. Input level shall be measured at the frame of the drive.

6.6.5 Operating Shock with E.S.P. Option

The drive withstands no damage under a half-sine wave shock pulse of 19600 m/sec2 of 1msec duration on six sides. All shocks shall be applied in each direction of the drive's three mutually perpendicular axes, one axis at a time. Input level shall be measured at frame of the drive. Shock shall be applied after a free-fall (0 – 3m/sec^2) condition with the E.S.P. sensitivity set meeting its fall height. Refer to section 11.10.21Set E.S.P. Threshold (8Ch) (Vendor Unique) for details on the sensitivity setting.

6.7 Acoustics

6.7.1 Sound Power Level

The criteria of A-weighted sound power level are described as follows.
Measurements are to be taken in accordance with ISO 7779. The mean of 40 drives is to be less than the typical value. Each drive is to be less than the maximum value. Drives are to meet this requirement in both board down orientations.

A-weighted sound power	Typical (Bels)	Maximum (Bels)
Idle	1.8	2.0
Operating	2.1	2.4

Table 16 Sound power levels

Background power levels of the acoustic test chamber for each octave band are to be recorded. Sound power tests are to be conducted with the drive supported by spacers so that the lower surface of the drive is located at 25+-3 mm height from the chamber floor. No sound absorbing material is used. The acoustical characteristics of the drive are measured under the following conditions:

Mode	Description
Idle	Power on, spindle motor spinning, track following, the drive ready to receive and respond to command immediately
Operating	Continuous random cylinder selection and seek operation of actuator with a dwell time at each cylinder. Seek rate for the drive can be calculated as follows: $N_S = 0.4 / (T_t+T_1)$ where, N_S = average seek rate in seeks/seconds T_t = published seek time from one random track to another without including rotational latency T_1 = equivalent time, in seconds, for the drive to rotate by half revolution

6.7.2 Discrete Tone Penalty

Discrete tone penalties are added to the A-weighted sound power with the following fomula only when determining compliance:

$LW_t(spec) = LW + 0.1P_t + 0.3 < 4.0$ (Bels)

where

LW = A-weighted sound power level

P_t = value of discrete tone penalty [= dL_t-6.0(dBA)]

dL_t = Tone-to-noise ratio taken in accordance with ISO 7779 at each octave band

6.8 Identification Labels

The labels are affixed to every drive.

The top side of the label contains

- Model name
- Part number
- The statement “made by Hitachi Global Storage Technologies”
- Country of origin
- The marks of Agencies approval
- Bar code of the serial number

The bottom side of the label contains

- The Hitachi Logo
- The capacity
- The product name (Microdrive®)

6.9 Electromagnetic compatibility

Hitachi will provide technical support to assist users in complying with the EMC requirements.

6.10 Safety

6.10.1 Underwriters Lab (UL) approval

All models of the drive comply with UL 1950.

6.10.2 Canadian Standards Authority (CSA) approval

All models of the drive comply with CSA C22.2 950-M1 1995.

6.10.3 IEC compliance

All models of the drive comply with IEC 950.

6.10.4 German Safety Mark

All models of the drive are approved by TUV on Test Requirement EN 60 950:1988/A1:1990, but the GS mark has not been obtained.

6.10.5 Flammability

Printed circuit boards used in the drive are made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components except for minor mechanical parts are made of material with a UL recognized flammability rating of V-x or better.

6.10.6 Safe Handling

The drives are designed for safe handling with regards to shape edges and corners.

6.10.7 Environment

The drive does not contain any known or suspected carcinogens.
Environmental controls meet or exceed all applicable government regulations in the county of origin. Safe chemical usage and manufacturing process used to build the drive, the drive itself, and the disposal of the drive at the end of its life.
Production also meets the requirements of the international treaty on chlorofluorocarbon (CFC) control known as the United Nations Environment Program Montreal Protocol, and as ratified by the member nations. Materials to be controlled include CFC-11, CFC-12, CFC-113, CFC-114, CFC-115, Halon 1211, Halon 1301, and Halon 2402. Although not specified by the protocol, CFC-112 is also controlled. In addition to the protocol Hitachi Global Storage Technologies requires the following:

- No packaging used for the shipment of the product uses controlled CFCs in the manufacturing process.
- No manufacturing process for parts or assemblies-including printed circuit boards-use controlled CFC materials.

6.10.8 Secondary circuit protection

The drive utilizes printed circuit wiring that must be protected against the possibility of sustained combustion due to circuit or component failures as defined in C-B 2-4700-034 (Protection Against Combustion). Adequate secondary over-current protection is responsibility of the using system. The user protects the drive from its electrical short circuit problem. A 0.5 Amp limit is required for safety purpose.

6.11 Packaging

The drives are shipped in appropriate containers and placed on pallets in accordance with Hitachi Global Storage Technologies Supplier Packaging Instruction.

The drives procured under this specification are assembled and tested using Electrostatic Discharge Protection process and procedure. A protection system suitable for the disk drive msut be installed and monitored by the appropriate ME/QA function. The goal is to prevent electrostatic potential from accumulating on any object which may deliberately or inadvertently be brought into contact with the drive.

The drives are shipped in ESD protective bags as defined in the Hitachi Global Storage Technologies speciation control drawing.

Part 2. Parallel ATA Interface Specification

7 Electrical Interface Specifications

The following table defines all the DC characteristics of the drive. Unless otherwise stated, the following are the electrical interface requirements:

- Vcc = 3.3 + 5/-15%
- Ta = 5 – 60 ˚C (60 ˚C Maximum at top cover of the drive)

(See section)

Symbol	Item	Measurement Method	Conditions	Units
V_{CC}	Input Power			Volts
V_I	Input Voltage			Volts
V_O	Output Voltage			Volts
P_d	Power Consumption	Ta = 25 ˚C		
T_{opr}	Operating Temperature		5 - 60	˚C
T_{stg}	Storage Temperature		-40 - 70	˚C

Table 17 DC Characteristics

7.1 Interface Connector

The drive implements 35 position 0.3mm pitch ZIF connector. See 6.5.3Connector.

7.2 Signal Definition

The pin assignments of the interface signals are shown in the following table.

Pin Num	Signal Name	Pin Type	I/O Type	Pin Num	Signal Name	Pin Type	I/O Type
1	GND		Ground	19	VCC		Power
2	DD10	I/O	TS-CIO	20	INTRQ	O	TS-OCD
3	DD9	I/O	TS-CIO	21	DIOW-	I	OCR
4	DD2	I/O	TS-CIO	22	DIOR- HDMARDY HSTORBE	I	OCR
5	DD8	I/O	TS-CIO	23	CS1-	I	OCR
6	DD1	I/O	TS-CIO	24	CS0-	I	OCR
7	PDIAG-	I/O	TS-OCD	25	DD15	I/O	TS-CIO
8	DD0	I/O	TS-CIO	26	DD7	I/O	TS-CIO
9	DASP-	I/O	TS-OCD	27	DD14	I/O	TS-CIO
10	DA0	I	OCR	28	DD6	I/O	TS-CIO
11	DMACK-	I	OCR	29	DD13	I/O	TS-CIO
12	DA1	I	OCR	30	DD5	I/O	TS-CIO
13	DMARQ	O	TS-OCD	31	DD12	I/O	TS-CIO
14	DA2	I	OCR	32	DD4	I/O	TS-CIO
15	IORDY DDMARDY- DSTROBE	O	TS-OCD	33	DD11	I/O	TS-CIO
16	RESET-	I	OCR	34	DD3	I/O	TS-CIO
17	CSEL-	I	OCR	35	GND		Ground
18	VCC		Power				

Notes:

"I" : designates an input to the drive

"O" : designates an output from the drive

"I/O" : designates an input/output common

TS = three-state, OCD = driver, OCR = receiver, CIO = bi-directional driver/receiver

Table 18 Signal Definition

7.3 Signal Description

Signal Name	Description
CS(1:0)	These are chip select signals from the host used to select the Command Block or Control Block registers. When DMACK- is asserted, the host shall negate CS0- and CS1 to ensure 16 bits data transfer.
CSEL	As a default shipping configuration, the device does not sample this signal and will be a DEVICE 0 regardless of the condition of this signal.
DA(2:0)	Address used to select the individual register in the device
DASP-	As a default shipping configuration, the device will not be a DEVICE 1. The device asserts this signal when active other than reset protocol.
DD(15:0)	16-bits bi-directional data bus between the host and the device. The lower 8 lines, DD(7:0) are used for Register and ECC access. All 16 lines, DD(15:0) are used for data transfer. These are 3-state bidirectional driver/receiver with 16mA current sink capability.
DIOR- HDMARDY HSTROBE	DIOR- is the strobe signal used by the host to read device registers or the Data port. Data is transferred on the negation of this signal. HDMARDY – is a flow control signal for Ultra DMA data-in bursts. This signal is asserted by the host to the device that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY- to pause an Ultra DMA data-in burst. HSTORBE is the data-out strobe signal from the host for an Ultra DMA data-out burst. Both the rising and falling edge of HSTROBE latch the data from DD(15:0) into the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
DIOW- STOP	DIOW- is the strobe signal used by the host to write registers or the Data port. Data is transferred on the negation of this signal. The host shall negate DIOW- prior to initiation of an Ultra DMA burst. Assertion of STOP by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst.
DMACK-	This signal is used by the host in response to DMARQ to initiate DMA transfers. For Multiword DMA transfers, the DMARQ/DMAACK- handshake is used to provide flow control during the transfer. For Ultra DMA, the DMARQ/DMACK- handshake is used to indicate when the function of interface signals changed.

Signal Name	Description
DMARQ	This signal is used for the device when the device is ready to transfer data to or from the host for DMA data transfers. For Multiword DMA transfers, the direction of data transfer is controlled by DIOR- and DIOW-. The device waits until the host asserts DMACK- before negating DMARQ and re-asserting DMARQ if there is more data to transfer. For Multiword DMA transfers, the DMARQ/DMAACK- handshake is used to provide flow control during the transfer. For Ultra DMA, the DMARQ/DMACK- handshake is used to indicate when the function of interface signals changed.
INTRQ	This signal is used by the selected device to interrupt the host system when Interrupt Pending Is set. When the nIEN bit is cleared to zero and the device is selected, the device enables INTRQ signal through a 3-state buffer. When the nIEN bit is set to one or the device is not selected, the device releases the signal.
IORDY DDMARDY- DSTROBE	The device will not negate IORDY signal to extend the host data transfer cycle for PIO mode 3 or above. However, it is recommended to host to support IORDY for PIO mode 3 or above data transfer speed. DDMARDY- is a flow control signal for Ultra DMA data-out bursts. The device asserts this signal to indicate to the host that the device is ready to receive Ultra DMA data-out burst. The device may negate DDMARDY- to pause an Ultra DMA data-out burst. DSTORBE is the data-in strobe signal from the device for an Ultra DMA data-in burst. Both the rising and falling edge of DSTROBE latch the data from DD(15:0) into the host. The device may stop generating DSTROBE edges to pause and Ultra DMA data-in burst.
PDIAG-	As a shipping default configuration, the device will only be a DEVICE 0 and will not sample PDIAG-, which may be asserted by DEVICE 1.
RESET-	This line is used to reset the drive. The reset caused by this signal is referred as hardware reset.

Table 19 Signal Descriptions

7.3.1 Interface logic signal levels

	Minimum (V)	Maximum (V)
Inputs		
Input High Voltage	2.0	
Input Low Voltage		0.8
Outputs		
Output High Voltage		2.4
Output Low Voltage	0.5	

Table 20 Interface logic signal levels

8 Interface Timing

8.1 PIO Mode Read/Write Timing Specification

The table below shows PIO mode Read/Write Timing.

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note
t0	Cycle time (min)	600	383	240	180	120	1
t1	Address Valid to -DIOR/-DIOW setup (min)	70	50	30	30	25	
t2	-DIOR/-DIOWR (min)	165	125	100	80	70	1
t2	-DIOR/-DIOW (min) Register (8 bit)	290	290	290	80	70	1
t2i	-DIOR/-DIOW recovery time (min)	-	-	-	70	25	
t3	-DIOW data setup (min)	60	45	30	30	20	
t4	-DIOW data hold (min)	30	20	15	10	10	
t5	-DIOR data setup (min)	50	35	20	20	20	
t6	-DIOR data hold (min)	5	5	5	5	5	
t6Z	-DIOR data tristate (max)	30	30	30	30	30	2
t9	-DIOR / -DIOW to address valid hold	20	15	10	10	10	
tRD	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0	
tA	IORDY Setup time	35	35	35	35	35	3
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
tC	IORDY assertion to release (max)	5	5	5	5	5	

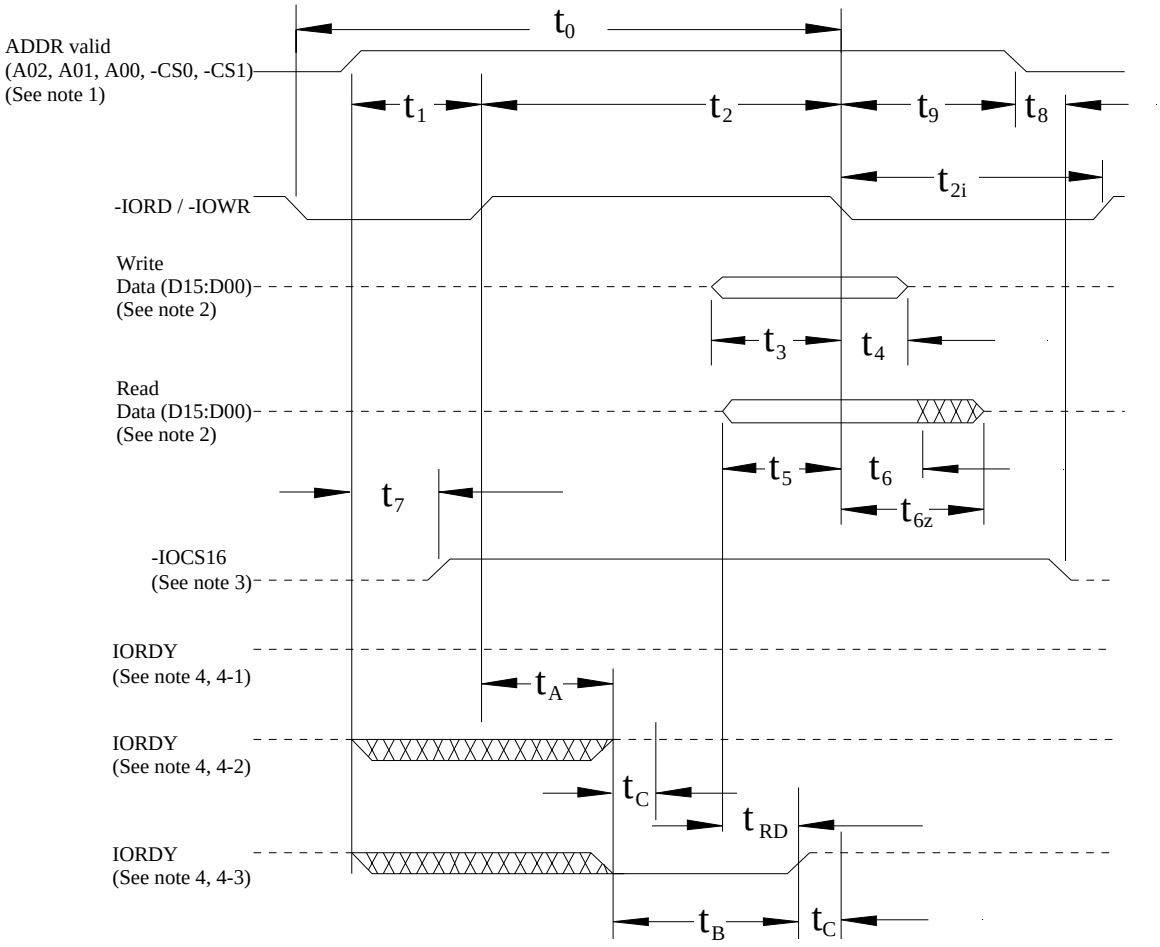
Notes:

All timings are in nanoseconds (nsec).

1. t0 is the minimum total cycle time, t2 is the minimum command active time, and t2i is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing

requirements of t0, t2, and t2i shall be met. The minimum total cycle time requirement is greater than the sum of t2 and t2i. This means a host implementation can lengthen either or both t2 or t2i to ensure that t0 is equal to or greater than the value reported in the device's identify device data.

2. This parameter specifies the time from the negation edge of -IORD to the time that the data bus is no longer driven by the device.
3. The delay from the activation of -DIOR or -DIOW until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at tA after the activation of -DIOR or -DIOW, then t5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time tA after the activation of -DIOR or -DIOW, then tRD shall be met and t5 is not applicable.
4. IORDY is not supported in this mode.



Notes:
(1) Device address consists of -CS0, -CS1, and A[02::00]
(2) Data consists of D[15::00] (16-bit) or D[07::00] (8 bit)
(3) -IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.
(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of -IORD or -IOWR. The assertion and negation of IORDY is described in the following three cases:
(4-1) Device never negates IORDY: No wait is generated.
(4-2) Device starts to drive IORDY low before tA, but causes IORDY to be asserted before tA: No wait generated.
(4-3) Device drives IORDY low before tA: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and -IORD is asserted, the device shall place read data on D15-D00 for tRD before causing IORDY to be asserted.

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Note)

The drive does not support –IOCS16 signal.

-DIOR/-DIOW are notated as –IORD/-IOWR respectively in the above figure.

Figure 1 PIO Mode Timing

8.2 Multiword DMA Timing Specification

The timing diagram for Multiword DMA mode of operation in this section is drawn using the conventions in the ATA-4 specification. Signals are shown with their asserted state as high regardless of whether the signal is actually negative or positive true. Consequently, the -DIOR, the -DIOW signals are shown in the diagram inverted from their electrical states on the bus.

	Item	Mode 0	Mode 1	Mode 2	Note
t_O	Cycle time (min)	480	150	120	1
t_D	-DIOR / -DIOW asserted width (min)	215	80	70	1
t_E	-DIOR data access (max)	150	60	50	
t_F	-DIOR data hold (min)	5	5	5	
t_G	-DIOR/-DIOW data setup (min)	100	30	20	
t_H	-DIOW data hold (min)	20	15	10	
t_I	DMACK to –DIOR/-DIOW setup (min)	0	0	0	
t_J	-DIOR / -DIOW to -DMACK hold (min)	20	5	5	
t_{KR}	-DIOR negated width (min)	50	50	25	1
t_{KW}	-DIOW negated width (min)	215	50	25	1
t_{LR}	-DIOR to DMARQ delay (max)	120	40	35	
t_{LW}	-DIOW to DMARQ delay (max)	40	40	35	
t_M	CS(1:0) valid to –DIOR / -DIOW	50	30	25	
t_N	CS(1:0) hold	15	10	10	
t_Z	-DMACK	20	25	25	

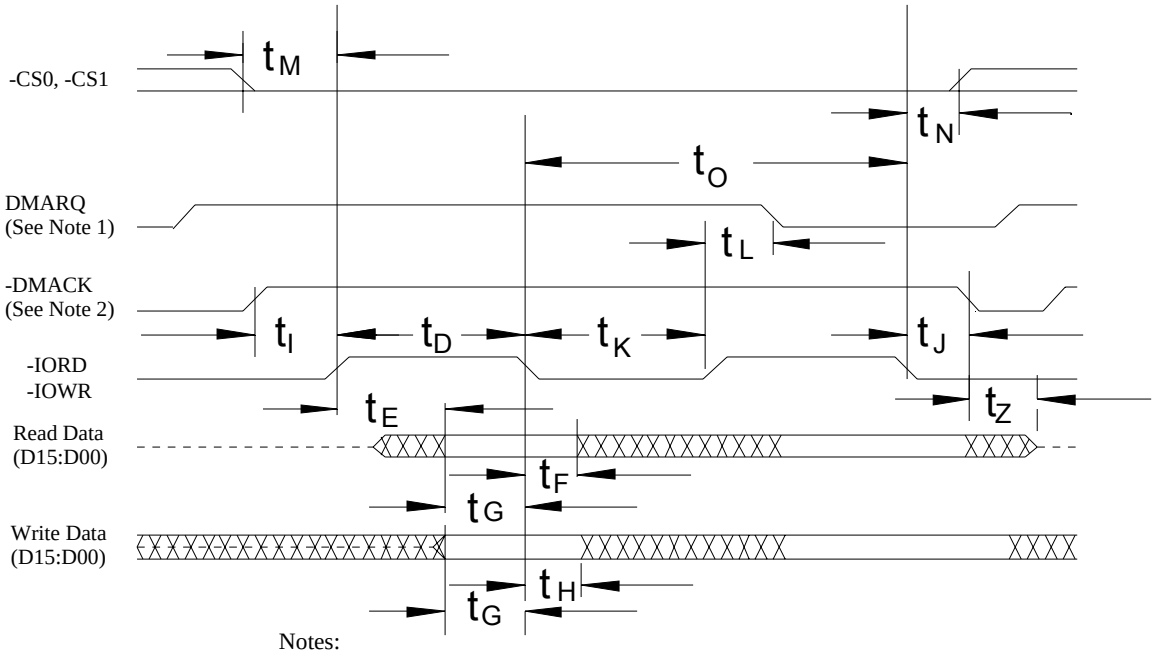
Notes:

All timings are in nanoseconds (nsec).

1. t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the

actual command inactive time. The three timing requirements of t_0, t_D, t_{KR}, and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW}.for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR}, and t_{KW} as needed to ensure that t_0 is equal to or greater than the value reported in the device's identify device data.

Table 21 Multiword DMA Timing Specification



Notes:

(1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.

(2) This signal may be negated by the host to suspend the DMA transfer in progress.

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes)

-DIOR/-DIOW are notated as –IORD/-IOWR respectively in the above figure.

Figure 2 Multiword DMA Timing

8.3 Ultra DMA Mode Timing Specification

8.3.1 Ultra DMA Overview

Ultra DMA is an optional data transfer protocol used with the READ DMA, and WRITE DMA, commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g.,Command Block Register access).

Several signal lines are redefined to provide different functions during an Ultra DMA burst. These lines assume these definitions when:

1. an Ultra DMA mode is selected, and
2. a host issues a READ DMA, or a WRITE DMA command requiring data transfer, and
3. the host asserts -DMACK.

These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of -DMACK by the host at the termination of an Ultra DMA burst.

With the Ultra DMA protocol, the STROBE signal that latches data from D[15:00] is generated by the same agent (either host or device) that drives the data onto the bus. Ownership of D[15:00] and this data strobe signal are given either to the device during an Ultra DMA data-in burst or to the host for an Ultra DMA data-out burst.

During an Ultra DMA burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data.

Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA mode at which the system operates. The Ultra DMA mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA mode shall be selected at any given time. All timing requirements for a selected Ultra DMA mode shall be satisfied. Devices supporting any Ultra DMA mode shall also support all slower Ultra DMA modes.

The device retains the previously selected Ultra DMA mode after executing a software reset sequence if a SET FEATURES disable reverting to defaults command has been issued. The device reverts to a Multiword DMA mode if a SET FEATURES enable reverting to default has been

issued. The device clears any previously selected Ultra DMA mode and reverts to the default non-Ultra DMA modes after executing a power-on or hardware reset.
Both the host and device perform a CRC function during an Ultra DMA burst. At the end of an Ultra DMA burst the host sends its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match, the device reports an error in the error register. If an error occurs during one or more Ultra DMA bursts for any one command, the device shall report the first error that occurred. If the device detects that a CRC error has occurred before data transfer for the command is complete, the device will complete the transfer and report the error.

8.3.2 Ultra DMA Phases of Operation

An Ultra DMA data transfer is accomplished through a series of Ultra DMA data-in or data-out bursts. Each Ultra DMA burst has three mandatory phases of operation: the initiation phase, the data transfer phase, and the Ultra DMA burst termination phase. In addition, an Ultra DMA burst may be paused during the data transfer phase. In the following rules -DMARDY is used in cases that could apply to either -DDMARDY or -HDMARDY, and STROBE is used in cases that could apply to either DSTROBE or HSTROBE. The following are general Ultra DMA rules.

1. An Ultra DMA burst is defined as the period from an assertion of -DMACK by the host to the subsequent negation of -DMACK.
2. When operating in Ultra DMA modes 2, 1, or 0 a recipient shall be prepared to receive up to two data words whenever an Ultra DMA burst is paused.

Ultra DMA Burst Initiation Phase Rules

An Ultra DMA burst initiation phase begins with the assertion of DMARQ by a device and ends when the sender generates a STROBE edge to transfer the first data word.

1. An Ultra DMA burst shall always be requested by a device asserting DMARQ.
2. When ready to initiate the requested Ultra DMA burst, the host shall respond by asserting -DMACK.
3. A host shall never assert -DMACK without first detecting that DMARQ is asserted.
4. For Ultra DMA data-in bursts: a device may begin driving D[15:00] after detecting that -DMACK is asserted, STOP negated, and -HDMARDY is asserted.
5. After asserting DMARQ or asserting -DDMARDY for an Ultra DMA data-out burst, a device shall not negate either signal until the first STROBE edge is generated.
6. After negating STOP or asserting -HDMARDY for an Ultra DMA data-in burst, a host shall not change the state of either signal until the first STROBE edge is generated.

Ultra DMA Data Transfer Phase Rules

1. The data transfer phase is in effect from after Ultra DMA burst initiation until Ultra DMA burst termination.
2. A recipient pauses an Ultra DMA burst by negating -DMARDY and resumes an Ultra DMA burst by reasserting -DMARDY.
3. A sender pauses an Ultra DMA burst by not generating STROBE edges and resumes by generating STROBE edges.
4. A recipient shall not signal a termination request immediately when the sender stops generating STROBE edges. In the absence of a termination from the sender the recipient shall always negate -DMARDY and wait the required period before signaling a termination request.
5. A sender may generate STROBE edges at greater than the minimum period specified by the enabled Ultra DMA mode. The sender shall not generate STROBE edges at less than the minimum period specified by the enabled Ultra DMA mode. A recipient shall be able to receive data at the minimum period specified by the enabled Ultra DMA mode.

Ultra DMA Data Transfer Phase Rules

1. Either a sender or a recipient may terminate an Ultra DMA burst.
2. Ultra DMA burst termination is not the same as command completion. If an Ultra DMA burst termination occurs before command completion, the command shall be completed by initiation of a new Ultra DMA burst at some later time or aborted by the host issuing a hardware or software reset or DEVICE RESET command if implemented by the device.
3. An Ultra DMA burst shall be paused before a recipient requests a termination.
4. A host requests a termination by asserting STOP. A device acknowledges a termination request by negating DMARQ.
5. A device requests a termination by negating DMARQ. A host acknowledges a termination request by asserting STOP.
6. Once a sender requests a termination, the sender shall not change the state of STROBE until the recipient acknowledges the request. Then, if STROBE is not in the asserted state, the sender shall return STROBE to the asserted state. No data shall be transferred on this transition of STROBE.
7. A sender shall return STROBE to the asserted state whenever the sender detects a termination request from the recipient. No data shall be transferred nor CRC calculated on this edge of DSTROBE.
8. Once a recipient requests a termination, the responder shall not change DMARDY from the negated state for the remainder of an Ultra DMA burst.
9. A recipient shall ignore a STROBE edge when DMARQ is negated or STOP is asserted.

8.3.3 Ultra DMA Data Transfer Timing

Name	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2		Measurement location
	Min(ns)	**Max(ns)**	**Min(ns)**	**Max(ns)**	**Min(ns)**	**Max(ns)**	
$t_{2CYCTYP}$	240		160		120		Sender
t_{CYC}	112		73		54		Note 3
t_{2CYC}	230		153		115		Sender
t_{DS}	15.0		10.0		7.0		Recipient
t_{DH}	5.0		5.0		5.0		Recipient
t_{DVS}	70.0		48.0		31.0		Sender
t_{DVH}	6.2		6.2		6.2		Sender
t_{CS}	15.0		10.0		7.0		Device
t_{CH}	5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		Host
t_{CVH}	6.2		6.2		6.2		Host
t_{ZFS}	0		0		0		Device
t_{DZFS}	70.0		48.0		31.0		Sender
t_{FS}		230		200		170	Device
t_{LI}	0	150	0	150	0	150	Note 4
t_{MLI}	20		20		20		Host
t_{UI}	0		0		0		Host
t_{AZ}		10		10		10	Note 5
t_{ZAH}	20		20		20		Host
t_{ZAD}	0		0		0		Device
t_{ENV}	20	70	20	70	20	70	Host
t_{RFS}		75		70		60	Sender
t_{RP}	160		125		100		Recipient
t_{IORDYZ}		20		20		20	Device
t_{ZIORDY}	0		0		0		Device
t_{ACK}	20		20		20		Host
t_{SS}	50		50		50		Sender

Notes:

1. All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
2. All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of tRFS, both STROBE and -DMARDY transitions are measured at the sender connector.
3. The parameter tCYC shall be measured at the recipient's connector farthest from the sender.
4. The parameter tLI shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.
5. The parameter tAZ shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.

Table 22 Ultra DMA Burst Timing Requirements

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until strobe edge)	2, 5
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2, 5
t_{DVS}	Data valid setup time at sender (from data valid until strobe edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1

Name	Comment	Notes
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

1. The parameters t_{UI}, t_{MLI} (in Figure 37:Ultra DMA data-In Burst Device Termination Timing and Figure 38:Ultra DMA Data-In Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.
2. 80-conductor cabling (see 8.6.3) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.
3. Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pf at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.
4. For all modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.
5. The parameters t_{DS}, and t_{DH} for mode 5 are defined for a recipient at the end of the cable only in a configuration with a single device located at the end of the cable. This could result in the minimum values for t_{DS} and t_{DH} for mode 5 at the middle connector being 3.0 and 3.9 ns respectively

Table 23 Ultra DMA Burst Timing Descriptions

Name	Comments	UDMA Mode 0		UDMA Mode 1		UDMA Mode 2	
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
t_{DSIC}	Recipient IC data setup time (from data valid until strobe edge) (see note 2)	14.7		9.7		6.8	
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)	4.8		4.8		4.8	
t_{DVSIC}	Sender IC data valid setup time (from data valid until STORBE edge) (see note 3)	72.9		50.9		33.9	
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)	9.0		9.0		9.0	

Notes:

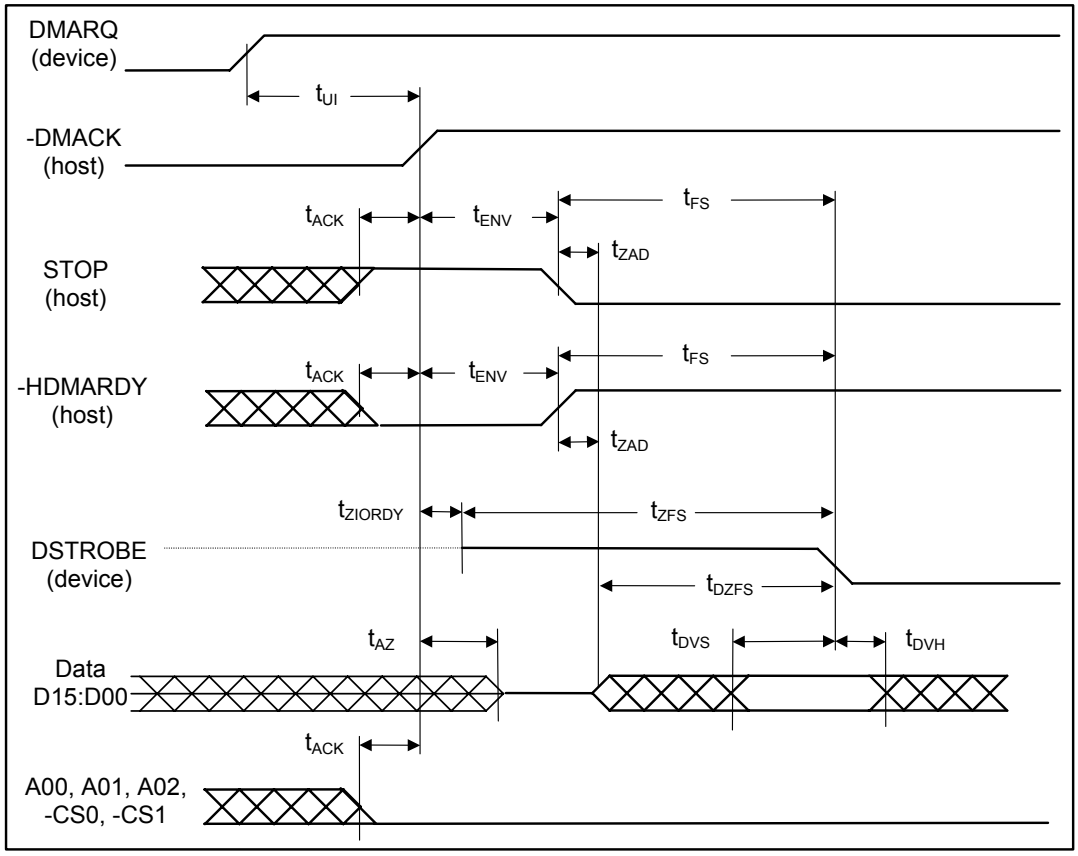
1. All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.
2. The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at t_{DSIC} and t_{DHIC} timing (as measured through 1.5 V).
3. The parameters t_{DVSIC} and t_{DVHIC} shall be met for lumped capacitive loads of 15 and 40 pf at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

Table 24 Ultra DMA Sender and Recipient IC Timing Requirements

Initiating Ultra DMA Data In Burst

An Ultra DMA Data-In burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 3 Ultra DMA Data-In Burst Initiation Timing. The associated timing parameters are specified in Table 22 Ultra DMA Burst Timing Requirements and are described in Table 23 Ultra DMA Burst Timing Descriptions. The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.
b) The device shall assert DMARQ to initiate an Ultra DMA burst.
c) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.
d) The host shall assert HSTROBE.
e) The host shall negate -CS0, -CS1, DA2, DA1, and DA0. The host shall keep -CS0, -CS1, DA2, DA1, and DA0 negated until after negating -DMACK at the end of the burst.
f) Steps (c), (d), and (e) shall have occurred at least tACK before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA burst.
g) The device may negate -DDMARDY tZIORDY after the host has asserted -DMACK. Once the device has negated -DDMARDY, the device shall not release -DDMARDY until after the host has negated DMACK at the end of an Ultra DMA burst.
h) The host shall negate STOP within tENV after asserting -DMACK. The host shall not assert STOP until after the first negation of HSTROBE.
i) The device shall assert -DDMARDY within tLI after the host has negated STOP. After asserting DMARQ and -DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.
j) The host shall drive the first word of the data transfer onto D[15:00]. This step may occur any time during Ultra DMA burst initiation.
k) To transfer the first word of data: the host shall negate HSTROBE no sooner than tUI after the device has asserted -DDMARDY. The host shall negate HSTROBE no sooner than tDVS after the driving the first word of data onto D[15:00].



Notes: The definitions for the IORDY:-DDMARDY:DSTROBE, -DIOR: -HDMARDY:HSTROBE, and -DIOW:STOP signal lines are not in effect until DMARQ and -DMACK are asserted.

Figure 3 Ultra DMA Data-In Burst Initiation Timing

Sustaining an Ultra DMA Data-In Burst

An Ultra DMA Data-In burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 4 Sustaining Ultra DMA Data-In Burst Timing. The timing parameters are specified in Table 22 Ultra DMA Burst Timing Requirements and are described in Table 23 Ultra DMA Burst Timing Descriptions.

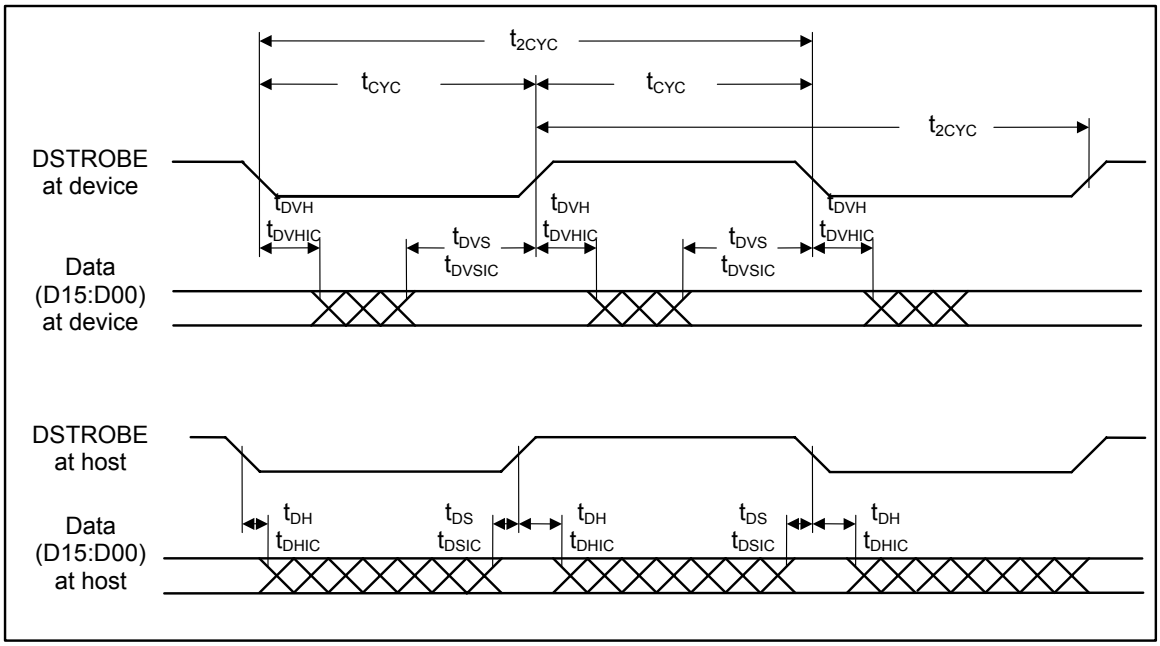
The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall drive a data word onto D[15:00].

b) The device shall generate a DSTROBE edge to latch the new word no sooner than tDVS after changing the state of D[15:00]. The device shall generate a DSTROBE edge no more frequently than tCYC for the selected Ultra DMA mode. The device shall not generate two rising or two falling DSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.

c) The device shall not change the state of D[15:00] until at least tDVH after generating a DSTROBE edge to latch the data.

d) The device shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.



Note: D[15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 4 Sustaining Ultra DMA Data-In Burst Timing

Host Pausing an Ultra DMA Data-In Burst

The host pauses a Data-In burst by following the steps lettered below. A timing diagram is shown in Figure 5 Ultra DMA Data-In Burst Host Pause Timing. The timing parameters are specified in Table 22 Ultra DMA Burst Timing Requirements and are described in Table 23 Ultra DMA Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

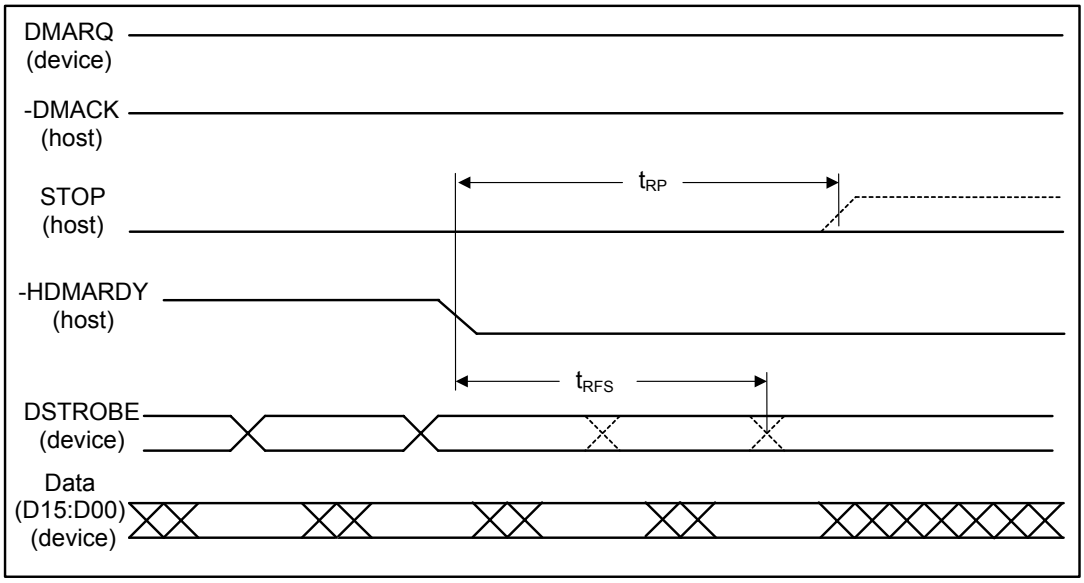
b) The host shall pause an Ultra DMA burst by negating -HDMARDY.

c) The device shall stop generating DSTROBE edges within tRFS of the host negating -HDMARDY.

d) If the host negates -HDMARDY within tSR after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host

negates -HDMARDY greater than tSR after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the device.

e) The host shall resume an Ultra DMA burst by asserting -HDMARDY.



Notes:

1. The host may assert STOP to request termination of the Ultra DMA burst no sooner than tRP after -HDMARDY is negated.
2. After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

Figure 5 Ultra DMA Data-In Burst Host Pause Timing

Device Terminating Ultra DMA Data-In Burst

The device terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 6 Ultra DMA Data-In Burst Device Terminating Timing. The timing parameters are specified in Table 22 Ultra DMA Burst Timing Requirements and are described in Table 23 Ultra DMA Burst Timing Descriptions

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

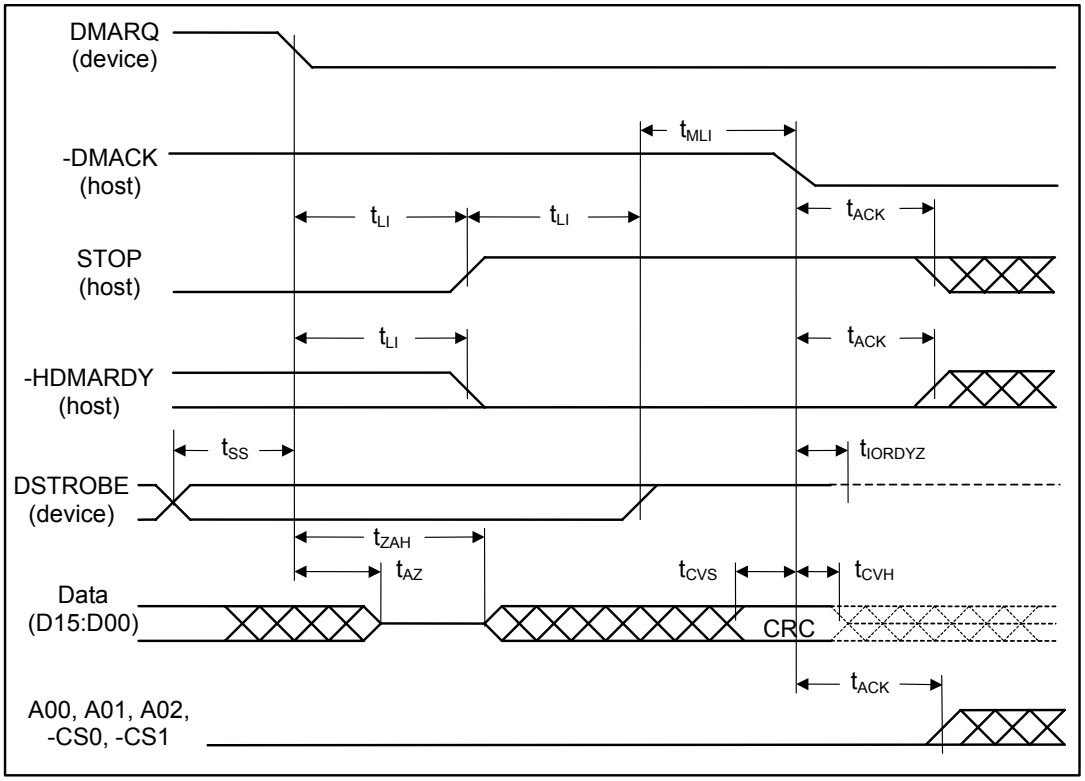
a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

b) The device shall pause an Ultra DMA burst by not generating DSTROBE edges.

c) NOTE-The host shall not immediately assert STOP to initiate Ultra DMA burst termination when the device stops generating STROBE edges. If the device does not negate DMARQ, in order to

initiate ULTRA DMA burst termination, the host shall negate -HDMARDY and wait tRP before asserting STOP.

d) The device shall resume an Ultra DMA burst by generating a DSTROBE edge.



Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 6 Ultra DMA Data-In Burst Device Terminating Timing

Host Terminating an Ultra DMA Data-In Burst

The host terminates an Ultra DMA Data-In burst by following the steps lettered below. The timing diagram is shown in Figure 7 Ultra DMA Data-In Burst Host Termination Timing. The timing parameters are specified in Table 22 Ultra DMA Burst Timing Requirements and are described in Table 23 Ultra DMA Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

b) The host shall initiate Ultra DMA burst termination by negating -HDMARDY. The host shall continue to negate -HDMARDY until the Ultra DMA burst is terminated.

c) The device shall stop generating DSTROBE edges within tRFS of the host negating -HDMARDY

d) If the host negates -HDMARDY within tSR after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDYgreater than tSR after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the device.

e) The host shall assert STOP no sooner than tRP after negating -HDMARDY. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

f) The device shall negate DMARQ within tLI after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

g) If DSTROBE is negated, the device shall assert DSTROBE within tLI after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.

h) The device shall release D[15:00] no later than t AZ after negating DMARQ.

i) The host shall drive DD D[15:00] no sooner than tZAH after the device has negated DMARQ. For this step, the host may first drive D[15:00] with the result of its CRC calculation.

j) If the host has not placed the result of its CRC calculation on D[15:00] since first driving D[15:00] during (9), the host shall place the result of its CRC calculation on D[15:00].

k) The host shall negate -DMACK no sooner than tMLI after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated -HDMARDY, and no sooner than tDVS after the host places the result of its CRC calculation on D[15:00].

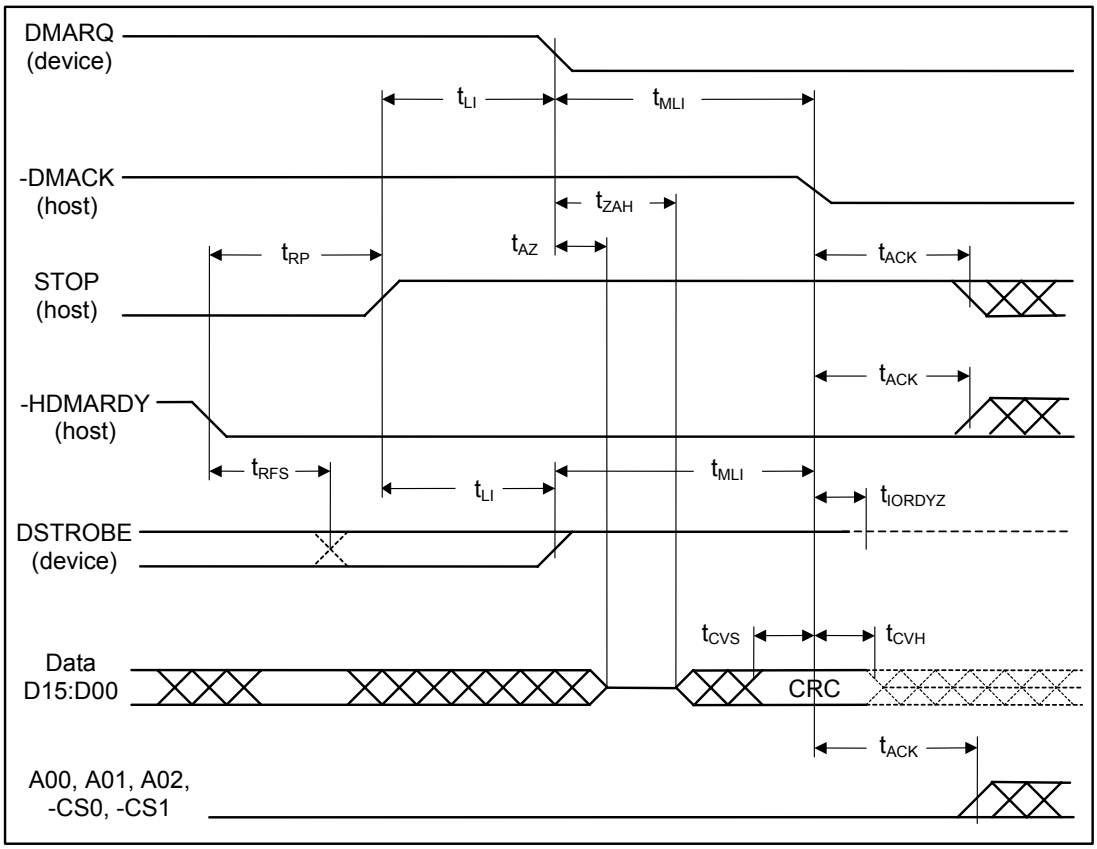
l) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

m) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA burst for any one command, at the end of the command, the device shall report the first error that occurred.

n) The device shall release DSTROBE within tIORDYZ after the host negates -DMACK.

o) The host shall neither negate STOP nor assert -HDMARDY until at least tACK after the host has negated -DMACK.

p) The host shall not assert -IORD, -CS0, -CS1, DA2, DA1, or DA0 until at least tACK after negating DMACK.



Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 7 Ultra DMA Data-In Burst Host Termination Timing

Initiating an Ultra DMA Data-Out Burst

An Ultra DMA Data-out burst is initiated by following the steps lettered below. The timing diagram is shown in Figure 8 Ultra DMA Data-Out Burst Initiation Timing. The timing parameters are specified in Table 22 Ultra DMA Burst Timing Requirements and are described in Table 23 Ultra DMA Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

q) The host shall keep -DMACK in the negated state before an Ultra DMA burst is initiated.

r) The device shall assert DMARQ to initiate an Ultra DMA burst.

s) Steps (c), (d), and (e) may occur in any order or at the same time. The host shall assert STOP.

t) The host shall assert HSTROBE.

u) The host shall negate -CS0, -CS1, DA2, DA1, and DA0. The host shall keep -CS0, -CS1, DA2, DA1, and DA0 negated until after negating -DMACK at the end of the burst.

v) Steps (c), (d), and (e) shall have occurred at least tACK before the host asserts -DMACK. The host shall keep -DMACK asserted until the end of an Ultra DMA burst.

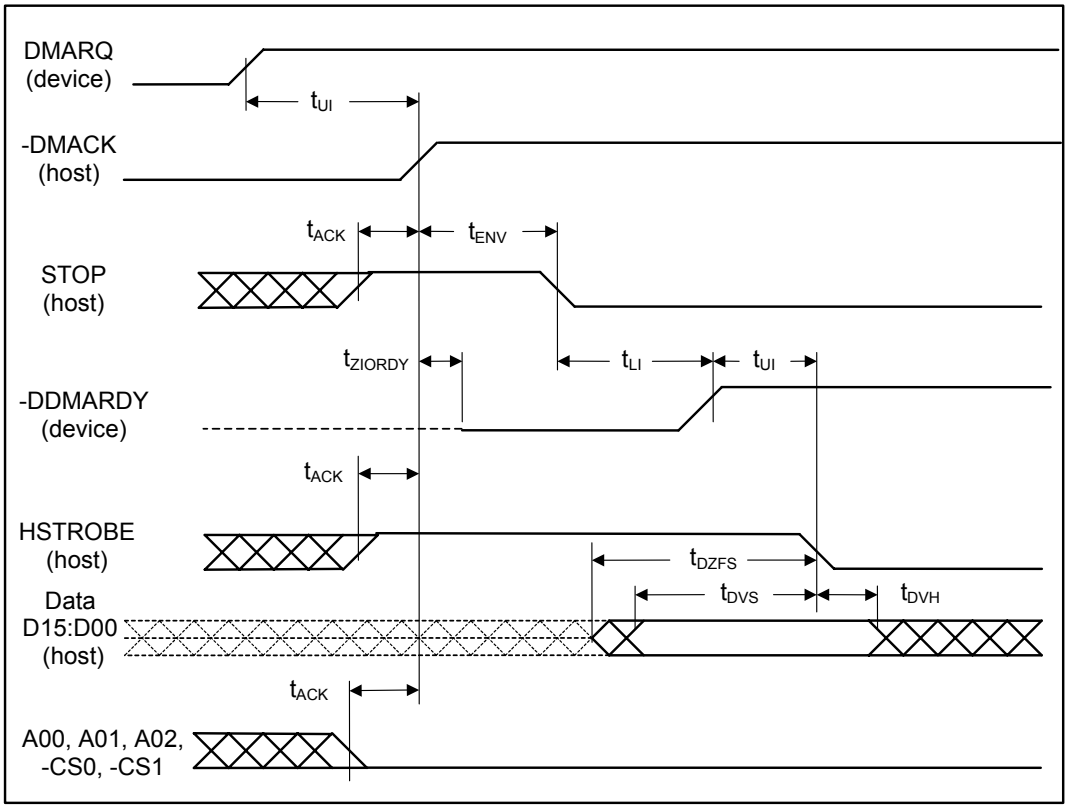
w) The device may negate -DDMARDY tZIORDY after the host has asserted -DMACK. Once the device has negated -DDMARDY, the device shall not release -DDMARDY until after the host has negated DMACK at the end of an Ultra DMA burst.

x) The host shall negate STOP within tENV after asserting -DMACK. The host shall not assert STOP until after the first negation of HSTROBE.

y) The device shall assert -DDMARDY within tLI after the host has negated STOP. After asserting DMARQ and -DDMARDY the device shall not negate either signal until after the first negation of HSTROBE by the host.

z) The host shall drive the first word of the data transfer onto D[15:00]. This step may occur any time during Ultra DMA burst initiation.

aa) To transfer the first word of data: the host shall negate HSTROBE no sooner than tUI after the device has asserted -DDMARDY. The host shall negate HSTROBE no sooner than tDVS after the driving the first word of data onto D[15:00].



Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

Figure 8 Ultra DMA Data-Out Burst Initiation Timing

Sustaining an Ultra DMA Data-Out Burst

An Ultra DMA Data-Out burst is sustained by following the steps lettered below. The timing diagram is shown in Figure 9 Sustaining an Ultra DMA Data-Out Burst. The associated timing parameters are specified in Table 22 Ultra DMA Burst Timing Requirements and are described in Table 23 Ultra DMA Burst Timing Descriptions.

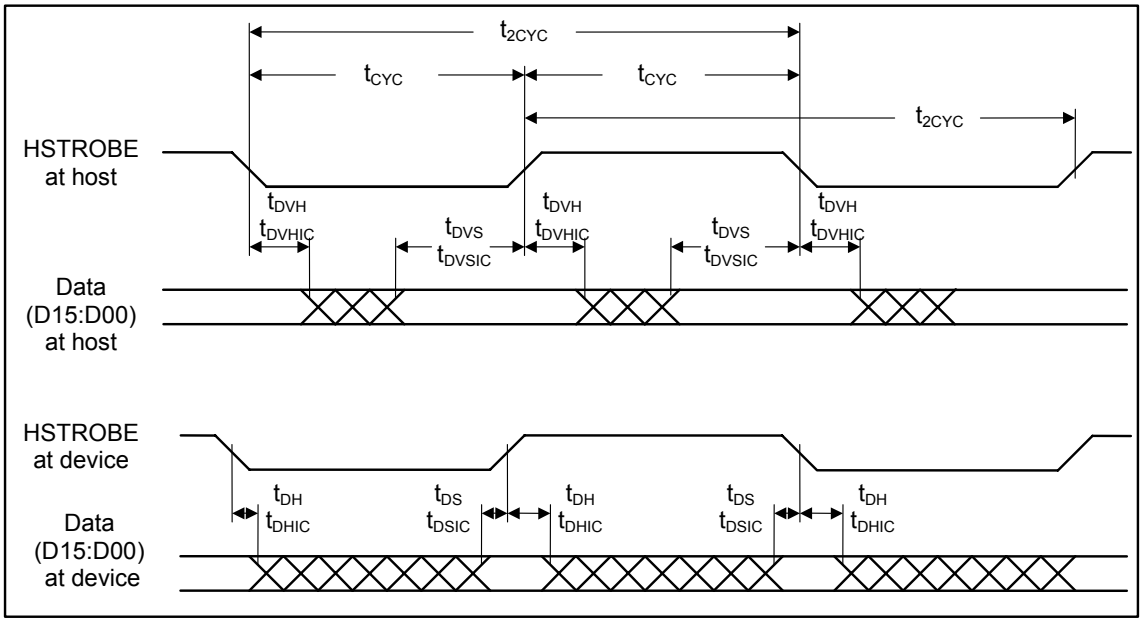
The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall drive a data word onto D[15:00].

b) The host shall generate an HSTROBE edge to latch the new word no sooner than tDVS after changing the state of D[15:00]. The host shall generate an HSTROBE edge no more frequently than tCYC for the selected Ultra DMA mode. The host shall not generate two rising or falling HSTROBE edges more frequently than 2tcyc for the selected Ultra DMA mode.

c) The host shall not change the state of D[15:00] until at least tDVH after generating an HSTROBE edge to latch the data.

d) The host shall repeat steps (a), (b), and (c) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.



Note: Data (D15:D00) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

Figure 9 Sustaining an Ultra DMA Data-Out Burst

Device Pausing an Ultra DMA Data-Out Burst

The device pauses an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram is shown in Figure 10 Ultra DMA Data-Out Burst Device Pause Timing. The timing parameters are specified in Table 22 Ultra DMA Burst Timing Requirements and are described in Table 23 Ultra DMA Burst Timing Descriptions

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.

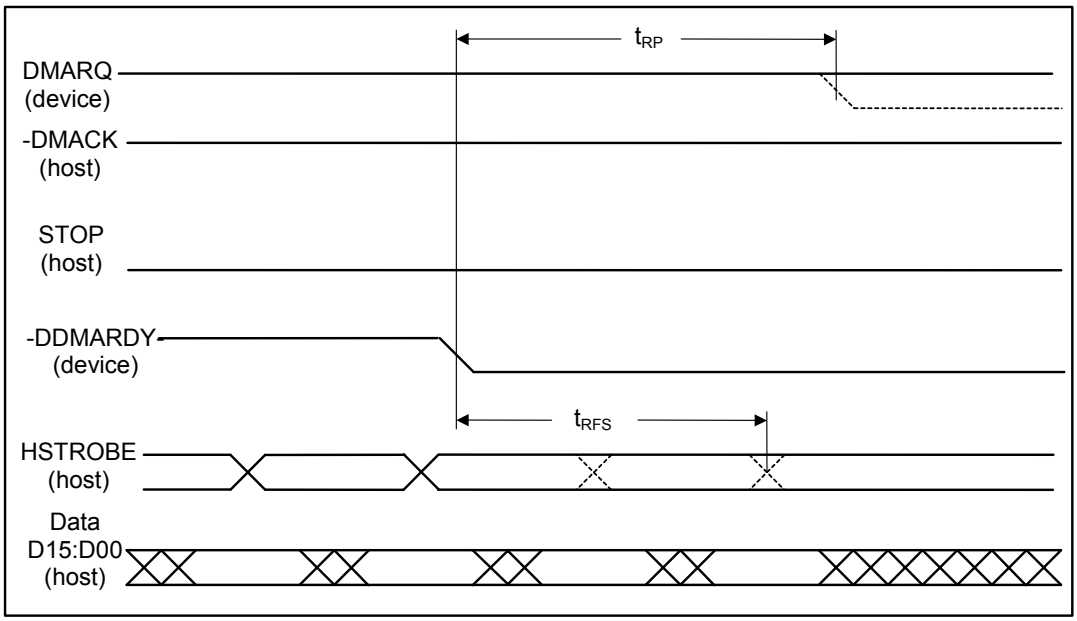
b) The device shall pause an Ultra DMA burst by negating -DDMARDY.

c) The host shall stop generating HSTROBE edges within tRFS of the device negating -DDMARDY.

d) If the device negates -DDMARDY within tSR after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than tSR after the host has generated an HSTROBE edge, then

the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the host.

e) The device shall resume an Ultra DMA burst by asserting -DDMARDY.



Notes:

1. The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than tRP after -DDMARDY is negated.
2. After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host.

Figure 10 Ultra DMA Data-Out Burst Device Pause Timing

Device Terminating an Ultra DMA Data-Out Burst

The device terminates an Ultra DMA Data-Out burst by following the steps lettered below. The timing diagram for the operation is shown in Figure 11 Ultra DMA Data-Out Burst Device Termination Timing. The timing parameters are specified in Table 22 Ultra DMA Burst Timing Requirements and are described in Table 23 Ultra DMA Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.

b) The device shall initiate Ultra DMA burst termination by negating -DDMARDY.

c) The host shall stop generating an HSTROBE edges within tRFS of the device negating -DDMARDY.

d) If the device negates -DDMARDY within tSR after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates -DDMARDY greater than tSR after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and tRFS timing for the host.

e) The device shall negate DMARQ no sooner than tRP after negating -DDMARDY. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

f) The host shall assert STOP within tLI after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

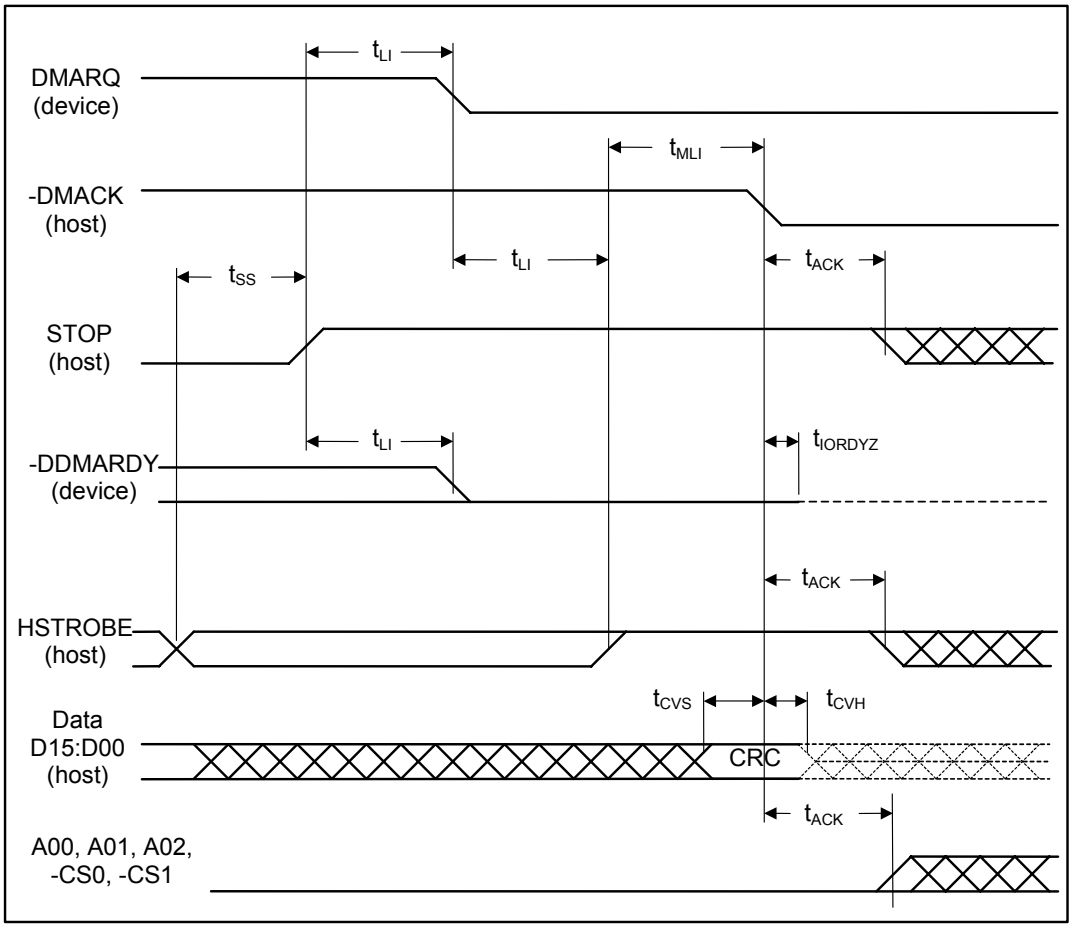
g) If HSTROBE is negated, the host shall assert HSTROBE within tLI after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.

h) The host shall place the result of its CRC calculation on D[15:00] .

i) The host shall negate -DMACK no sooner than tMLI after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than tDVS after placing the result of its CRC calculation on D[15:00].

j) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

k) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command.



Note: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 11 Ultra DMA Data-Out Burst Device Termination Timing

Host Terminating an Ultra DMA Data-Out Burst

Termination of an Ultra DMA Data-Out burst by the host is shown in Figure 12 Ultra DMA Data-Out Burst Host Termination Timing. Ultra DMA Data-Out Burst Host Termination Timing while timing parameters are specified in Table 22 Ultra DMA Burst Timing Requirements and are described in Table 23 Ultra DMA Burst Timing Descriptions.

The following steps shall occur in the order they are listed unless otherwise specifically allowed:

a) The host shall initiate termination of an Ultra DMA burst by not generating HSTROBE edges.

b) The host shall assert STOP no sooner than tSS after it last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.

c) The device shall negate DMARQ within tLI after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.

d) The device shall negate -DDMARDY within tLI after the host has negated STOP. The device shall not assert -DDMARDY again until after the Ultra DMA burst termination is complete.

e) If HSTROBE is negated, the host shall assert HSTROBE within tLI after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.

f) The host shall place the result of its CRC calculation on D[15:00].

g) The host shall negate -DMACK no sooner than tMLI after the host has asserted HSTROBE and STOP and the device has negated DMARQ and -DDMARDY, and no sooner than tDVS after placing the result of its CRC calculation on D[15:00].

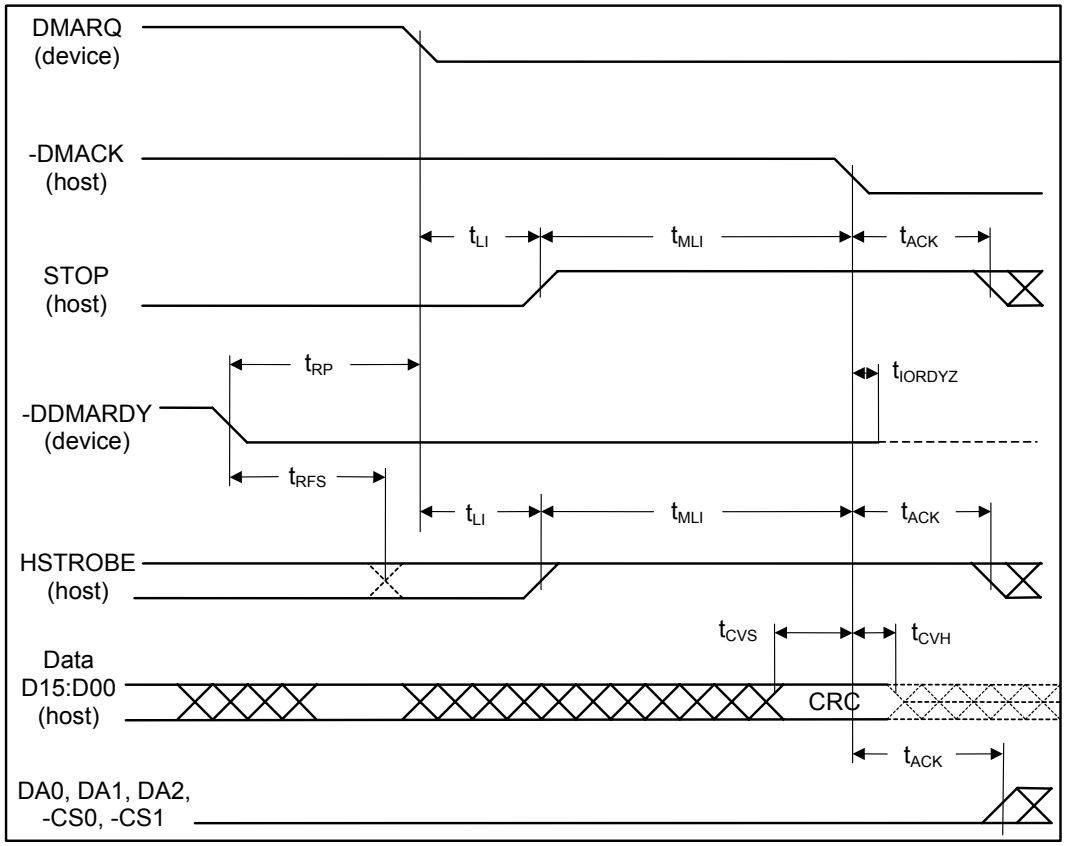
h) The device shall latch the host's CRC data from D[15:00] on the negating edge of -DMACK.

i) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.

j) The device shall release -DDMARDY within t IORDYZ after the host has negated -DMACK.

k) The host shall neither negate STOP nor negate HSTROBE until at least tACK after negating -DMACK.

l) The host shall not assert -IOWR, -CS0, -CS1, DA2, DA1, or DA0 until at least tACK after negating -DMACK.



Notes: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 12 Ultra DMA Data-Out Burst Host Termination Timing

Ultra DMA CRC Calculation

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA burst, and reporting any error that occurs at the end of a command.

1. Both the host and the device shall have a 16-bit CRC calculation function.
2. Both the host and the device shall calculate a CRC value for each Ultra DMA burst.
3. The CRC function in the host and the device shall be initialized with a seed of 4ABAh at the beginning of an Ultra DMA burst before any data is transferred.
4. For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA burst termination request has been acknowledged.

5. At the end of any Ultra DMA burst the host shall send the results of its CRC calculation function to the device on D[15:00] with the negation of -DMACK.
6. The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error and report it at the end of the command. A subsequent Ultra DMA burst for the same command that does not have a CRC error shall not clear an error saved from a previous Ultra DMA burst in the same command. If a miscompare error occurs during one or more Ultra DMA bursts for any one command, at the end of the command, the device shall report the first error that occurred.
7. For READ DMA or WRITE DMA, commands: When a CRC error is detected, it shall be reported by setting both ICRC and ABRT (bit 7 and bit 2 in the Error register) to one. ICRC is defined as the “Interface CRC Error” bit. The host shall respond to this error by re-issuing the command.
8. A host may send extra data words on the last Ultra DMA burst of a data out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A device may have already received more data words than were required for the command. These extra words are used by both the host and the device to calculate the CRC, but, on an Ultra DMA data out burst, the extra words shall be discarded by the device.
9. The CRC generator polynomial is: G(X) = X16 + X12 + X5 + 1. Table 28 describes the equations for 16-bit parallel generation of the resulting polynomial (based on a word boundary).

NOTE:

˜ Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinational logic is then equivalent to shifting sixteen bits serially through the generator polynomial where D00 is shifted in first and D15 is shifted in last.

CRCIN0 = f16	CRCIN8 = f8 XOR f13
CRCIN1 = f15	CRCIN9 = f7 XOR f12
CRCIN2 = f14	CRCIN10 = f6 XOR f11
CRCIN3 = f13	CRCIN11 = f5 XOR f10
CRCIN4 = f12	CRCIN12 = f4 XOR f9 XOR f16
CRCIN5 = f11 XOR f16	CRCIN13 = f3 XOR f8 XOR f15
CRCIN6 = f10 XOR f15	CRCIN14 = f2 XOR f7 XOR f14
CRCIN7 = f9 XOR f14	CRCIN15 = f1 XOR f6 XOR f13
f1 = D00 XOR CRCOUT15	f9 = D08 XOR CRCOUT7 XOR f5
f2 = D01 XOR CRCOUT14	f10 = D09 XOR CRCOUT6 XOR f6
f3 = D02 XOR CRCOUT13	f11 = D10 XOR CRCOUT5 XOR f7
f4 = D03 XOR CRCOUT12	f12 = D11 XOR CRCOUT4 XOR f1 XOR f8
f5 = D04 XOR CRCOUT11 XOR f1	f13 = D12 XOR CRCOUT3 XOR f2 XOR f9
f6 = D05 XOR CRCOUT10 XOR f2	f14 = D13 XOR CRCOUT2 XOR f3 XOR f10
f7 = D06 XOR CRCOUT9 XOR f3	f15 = D14 XOR CRCOUT1 XOR f4 XOR f11
f8 = D07 XOR CRCOUT8 XOR f4	f16 = D15 XOR CRCOUT0 XOR f5 XOR f12

Notes:

1. f=feedback
2. D[15:0]=Data to or from the bus
3. CRCOUT = 16 bit edge triggered result (current CRC)
4. CRCOUT[15:0] are sent on matching order bits of D[15:0]

Table 25 Equations for parallel generation of an Ultra DMA CRC

An example of a CRC generator implementation is provided below in Figure 13 Ultra DMA Parallel CRC Generator Example.

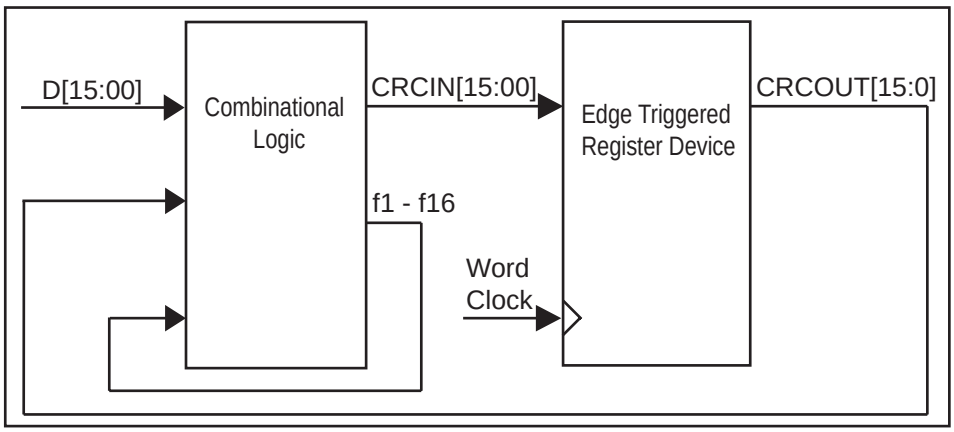


Figure 13 Ultra DMA Parallel CRC Generator Example

9 Parallel ATA Command Protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.
For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands, the host must also wait for RDY=1 before proceeding.
A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.
A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.
Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

9.1 PIO Data In Commands

These commands are;

- Identify Device
- Read Buffer
- Read Long
- Read Multiple
- Read Sectors

Execution includes the transfer of one or more 512byte (>512 bytes on Read Long) sectors of data from the device to the host.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. For each sector (or block) of data to be transferred:
    a. The device sets BSY=1 and prepares for data transfer.
    b. When a sector (or block) of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.

c. In response to the interrupt, the host reads the Status Register.

d. The device clears the interrupt in response to the Status Register being read.

e. The host reads one sector (or block) of data via the Data Register.

f. The device sets DRQ=0 after the sector (or block)has been transferred to the host.

4. For the Read Long command:

a. The device sets BSY=1 and prepares for data transfer.

b. When the sector of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.

c. In response to the interrupt, the host reads the Status Register.

d. The device clears the interrupt in response to the Status Register being read.

e. The host reads the sector of data including ECC bytes via the Data Register.

f. The device sets DRQ=0 after the sector has been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.
Note that the status data for a sector of data is available in the Status Register before the sector is transferred to the host.
If the device detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.
If an error occurs, the device will set BSY=0, ERR=1, and DRQ=1. The device will then store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The error location will be reported with CHS mode or LBA mode, the mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.
If an Uncorrectable Data Error (UNC=1) occurs, the defective data will be transferred from the media to the sector buffer, and will be available to be transferred to the host, at the host's option. In case of Read Multiple command, the host should complete transfer the block which includes the error from the sector buffer and terminate whatever kind of type of error occurred.
All data transfers to the host through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

9.2 PIO Data Out Commands

These commands are;

- Format Track
- Write Buffer
- Write Long
- Write Multiple
- Write Sectors
- Write Verify

Execution includes the transfer of one or more 512 bytes (>512 bytes on Write Long) sectors of data from the host to the device.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. For each sector (or block) of data to be transferred:
    a. The device sets BSY=0 and DRQ=1 when it is ready to receive a sector (or block).
    b. The host writes one sector (or block) of data via the Data Register.
    c. The device sets BSY=1 after it has received the sector (or block).
    d. When the device has finished processing the sector (or block), it sets BSY=0, and interrupts the host.
    e. In response to the interrupt, the host reads the Status Register.
    f. The device clears the interrupt in response to the Status Register being read.
5. For the Write Long command:
    a. The device sets BSY=0 and DRQ=1 when it is ready to receive a sector.
    b. The host writes one sector of data including ECC bytes via the Data Register.
    c. The device sets BSY=1 after it has received the sector.
    d. After processing the sector of data the device sets BSY=0 and interrupts the host.
    e. In response to the interrupt, the host reads the Status Register.
    f. The device clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.
If the device detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.
If an uncorrectable error occurs, the device will set BSY=0 and ERR=1, store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The error location will be reported with CHS mode or LBA mode. The mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.
All data transfers to the device through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

9.3 Non-Data Commands

These commands are;

- Check Power Mode
- Execute Device Diagnostic
- Flush Cache
- Format Unit
- Idle
- Idle Immediate
- Initialize Device Parameters
- Read Verify Sectors
- Recalibrate
- Security Erase Prepare
- Seek
- Sense Condition
- Set Features
- Set Multiple Mode
- Sleep
- Standby
- Standby Immediate

Execution of these commands involves no data transfer.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Device/Head Registers
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. When the device has finished processing the command, it sets BSY=0, and interrupts the host.
5. In response to the interrupt, the host reads the Status Register
6. The device clears the interrupt in response to the Status Register being read.

9.4 DMA Data Transfer Commands

These commands are;

- Read DMA
- Write DMA

Data transfer using DMA commands differ in two ways from PIO transfers:

- data transfers are performed using the slave-DMA channel.
- no intermediate sector interrupts are issued on multi-sector commands.

Initiation of the DMA transfer commands is identical to the Read Sectors or Write Sectors commands except that the host initializes the slave-DMA channel prior to issuing the command.
The interrupt handler for DMA transfers is different that:

- no intermediate sector interrupts are issued on multi-sector commands.
- the host resets the DMA channel prior to reading status from the device.

The DMA protocol allows high performance multi-tasking operating system to eliminate processor overhead associated with PIO transfer.

1. The host initializes the slave-DMA channel.
2. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Device/Head Registers
3. The host writes the command code to the Command Register.
4. The device sets DMARQ when it is ready to transfer any part of the data.
5. Host transfers the data using the DMA transfer protocol currently in effect.
6. When all of the data has been transferred, the device generates an interrupt to the host.

6 Host resets the slave-DMA channel

7 Host reads the Status Register and, and optionally the Error Register

Part.3 Logical Specification

10 ATA Register Description

10.1 ATA Registers

10.1.1 ATA Registers address

The Command Block registers are used for sending commands to the device or posting status from the device.

The Control Block registers are used for device control and to post alternate status.

-CS1	-CS0	DA2	DA1	DA0	-DIOR=0	-DIOW=0
1	0	0	0	0	RD Data	WR Data
1	0	0	0	1	Error	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector Number	Sector Number
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Device/Head	Device/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alternate Status	Device Control
0	1	1	1	1	Device Address	Reserved

Figure 14 ATA Registers Address

10.1.2 Alternate Status Register

Alternate Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR

Figure 15 Alternate Status Register

This register contains the same information as the Status Register. The only difference is that reading this register does not imply interrupt acknowledge or clear a pending interrupt.

10.1.3 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written.
All other registers required for the command must be set up before writing the Command Register.

10.1.4 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.
In LBA Mode this register contains Bits 16-23. At the end of the command, this register is updated to reflect the current LBA Bits 16-23.
The cylinder number may be from zero to the number of cylinders minus one.

10.1.5 Cylinder Low Register

This register contains the low order 8 bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.
In LBA Mode this register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15.
The cylinder number may be from zero to the number of cylinders minus one.

10.1.6 Data Register

This register is used to transfer data blocks between the device data buffer and the host for data-in, data-out and DMA commands.

10.1.7 Device Control Register

Device Control Register							
7	6	5	4	3	2	1	0
-	-	-	-	1	SRST	-IEN	0

Figure 16 Device Control Register

This register is used to control the device interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY.

Bit Definitions	
SRST (RST)	Software Reset. The device is held reset when RST=1. Setting RST=0 re-enables the device. The host must set RST=1 and wait for at least 5 microseconds before setting RST=0, to ensure that the device recognizes the reset.
-IEN	Interrupt Enable. When -IEN=0, and the device is selected, device interrupts to the host will be enabled. When -IEN=1, or the device is not selected, device interrupts to the host will be disabled.

10.1.8 Device Head Register

Device/Head Register							
7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

Figure 17 Device Head Register

This register contains the device and head numbers

Bit Definitions	
L	Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.
DRV	Device. When DRV=0, device 0 (master) is selected. When DRV=1, device 1 (slave) is selected.
HS3,HS2,HS1,HS0	Head Select. These four bits indicate binary encoded address of the head. HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head. The head number may be from zero to the number of heads minus one. In LBA mode, HS3 through HS0 contain bits 24-27 of the LBA. At command completion, these bits are updated to reflect the current LBA bits 24-27.

10.1.9 Error Register

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

Figure 18 Error Register

This register contains status from the last command executed by the device, or a diagnostic code. At the completion of any command except Execute Device Diagnostic, the contents of this register are valid always even if ERR=0 in the Status Register.
Following a power on, a reset, or completion of an EXECUTE DEVICE DIAGNOSTICS command, this register contains a diagnostic code.

11 General Operational Descriptions

11.1 Reset Response

There are three types of resets in a device: a power-on reset, a hardware reset, and a software reset.

Type	Description
Power On Reset (POR)	A reset carried out upon device's every power up sequence
Hard Reset (Hardware Reset)	A reset initiated by a raising edge of RESET signal (in True IDE mode)
Soft Reset (Software Reset)	A reset initiated by changing bit 2 (SRST) of Device Control Register as 0, 1 then 0

Table 26 Reset Type

The table below shows detailed effects on the device of each type of resets.

Description	POR	Hard Reset	Soft Reset
Aborting Host interface	–	0	0
Aborting Device operation	–	'(1)	'(1)
Initialization of hardware	0	0	X
Internal diagnostics	0	0	X
Initialization of task file registers (2)	0	0	0
Initialization of registers at attribute memory	0	0	X
DASP– handshake (3)	0	0	0
PDIAG– handshake (3)	0	0	0
Reverting programmed parameters to power-on default	0	0	'(4)
Logical geometry (number of cylinders/heads/sectors)			
Multiple mode			
Write cache			
Read look-ahead			
ECC bytes for Read Long and Write Long			
Delayed Write			
On-demand prefetch			
Byte transfer mode (3)			
PIO transfer mode			
DMA transfer mode (3)			
ABLE mode			
Reset Standby timer	0	0	X

Notes:

– - not applicable

O - executed

X - not executed

(1) If the device receives a reset during cached writing, the reset completes after cached writing completes.

(2) Initialized value of task file registers are shown in figure 58 below.

(3) True IDE mode only.

(4) If the device has received Set Features with feature code CCh prior to a reset, setting is reverted to the power-on default.

Table 27 Reset Response

11.1.1 Register Initialization

After Power on, hard reset or software reset, the register values are initialized as shown in the following table.

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	00h
Status	50h
Alternate Status	50h

Table 28 Default Register Values

The meaning of the Error Register diagnostic codes resulting from power on, hard reset or the EXECUTE DEVICE DIAGNOSTICS command are shown in the following table.

Code	Description
01h	No error Detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Device 1 failed

Table 29 Diagnostic Codes

11.2 Power-off considerations

11.2.1 Load/Unload

The drive supports a minimum of 300,000 normal load/unloads. The load/unload is a functional mechanism of the HDD. It is controlled by the drive firmware. Specifically, unloading of the head is invoked by the commands.

11.2.2 Emergency unload

When HDD power is interrupted while the heads are still loaded, the drive firmware can not operate and the normal 3.3V power is unavailable to unload the heads. In this case, normal controlled unload is not possible, the heads are unloaded by the current charge in capacitors on the drive. The actuator velocity is greater than the normal case, and the unload process is inherently less controllable without a normal seek current profile.
Emergency unload is intended to be invoked in rare situations. Because this operation is inherently uncontrolled, it is more mechanically stressful than a normal unload.

11.2.3 Required power-off sequence

Problems can occur on most HDDs when power is removed at an arbitrary time. Examples;

1. Data loss from the write buffer
2. If the drive is writing (a) sector(s), (a) partially-written sector(s) with an incorrect ECC block remain(s).

It is recommended to use the following sequence to avoid these problems to occur.

1. Issue STANDBY IMMEDIATE command (STANDBY IMMEDIATE command can be replaced by STANDBY or SLEEP command).
2. Wait until command complete status is returned. (It may take typically 500msec)
3. Terminate power to HDD

This power-down sequence should be followed for entry into any system power-down state, system suspend state or system hibernation state. In a robustly designed system, emergency unload is limited to rare scenarios such as battery removal during operation.

11.3 Sector Addressing Mode

11.3.1 Logical CHS Addressing Mode

The logical CHS addressing is made up of three fields: the cylinder number, the head number and the sector number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but can not exceed 255 (0xFF). Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode but can not exceed 15 (0xF). Cylinders are number from 0 to the maximum value allowed by the current CHS translation mode but can not exceed 65535 (0xFFFF).
When the host selects a CHS translation mode using the INITIALIZE DRIVE PARAMETERS command, the host requests the number of sector per logical track and the number of head per logical cylinder. The device then computes the number of logical cylinders available in requested mode. The current CHS translation mode, as well as the default CHS translation mode, is returned by the Identify Device Information.

11.3.2 LBA Addressing Mode

Logical sectors on the device is linearly mapped with the first LBA addressed sector (sector 0) being the same as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following is always true;

LBA =((cylinder*(heads per cylinder)+heads)*(sectors per track))+sector-1
Where (heads per cylinder) and (sectors per track) are the current translation mode values.
On LBA addressing mode, the LBA value is set to the following register

Device/Head	**<---**	LBA bits	27-24
Cylinder High	**<---**	LBA bits	23-16
Cylinder Low	**<---**	LBA bits	15- 8
Sector Number	**<---**	LBA bits	7- 0

11.4 Power Management Feature

The power management feature set permits a host to modify the behavior in a manner which reduces the power required to operate. The power management feature set provides a set of commands and a timer that enables a drive to implement low power consumption modes. The drive implements the following set of functions.

1. A Standby Timer
2. IDLE Command
3. IDLE IMMEDIATE Command
4. STANDBY Command
5. STANDBY IMMEDIATE Command

11.4.1 Power Mode

Standby Mode	The device interface is capable of accepting commands, but as the media may not immediately accessible, there is a delay while waiting for the spindle to reach operating speed.
Idle Mode	Refer to the section of Adoptive Battery Life Extender Feature.
Active Mode	The device is in execution of a command or accessing the disk media with read look-ahead function or write cache function.

11.4.2 Power Management Commands

The CHECK POWR MODE command allows a host to determine if a device is currently in, going to or leaving standby mode.

The IDLE and IDLE IMMEDIATE commands move a device to idle mode immediately from the active or standby modes.

The IDLE command also sets the standby timer count and starts the standby timer.

The STANDBY and STANDBY IMMEDIATE commands moves a device to standby mode immediately from the active or idle modes. The STANDBY command also sets the standby timer count.

11.4.3 STANDBY command completion timing

1. Confirm the completion of writing cached data in the buffer to media

2. Unload heads on the ramp
3. Set DRDY bit and DSC bit in Status Register
4. Set INTRQ (completion of the command)
5. Activate the spindle break to stop the spindle motor
6. Wait until spindle motor is stopped
7. Perform post process

11.4.4 Standby Timer

The standby timer provides a method for the device to automatically enter standby mode from either active or idle mode following a host programmed period of inactivity. If the device is in the active or idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the standby mode.
If the value of SECTOR COUNT Register on IDLE command or STANDBY command is set to 0x00, the device will automatically set the standby timer to 109 minutes. If the advanced power management level is less than 0x80, which is power-on default, the transition timing to enter Standby mode is determined by either standby timer or Adaptive Battery Life Extender algorithm, whichever meets the condition first.

11.4.5 Status

In the active, idle and standby modes, the device sets RDY it of the status register. If BSY bit is not set, the device is ready to accept any command.

11.4.6 Interface Capability for Power Modes

Each power mode affects the physical interface as defined in the following table:

Mode	BSY	RDY	Interface active	Media
Active	x	x	Yes	Active
Idle	0	1	Yes	Active
Standby	0	1	Yes	Inactive
Sleep	0	1	Yes	Inactive

Table 30 Power Conditions

Ready (RDY) bit in status register is not a power condition. The device may post ready at the interface even though the media may not be accessible.

11.4.7 Initial Power Mode at Power On

The device powers up in Standby mode.

11.5 Advanced Power Management Feature

This feature provides power saving without performance degradation. The **Adaptive Battery Life Extender 3 (ABLE-3)** technology intelligently manages transition among power modes within the device by monitoring access patterns of the host. This technology has three idle modes; Performance Idle mode, Active Idle mode and Low Power Idle mode.

This feature allows the host to select an advanced power management level. The advanced power management level is a scale from the lowest power consumption setting of 0x1 to the maximum performance level of 0xFE. Device performance may increase with increasing advanced power management levels. Device power consumption may increase with increasing advanced power management levels. The advanced power management levels contain discrete bands, described in the section of SET FEATURE command in detail. This feature set uses the following functions:
A SET FEATURES subcommand to enable Advanced Power Management
A SET FEATURES subcommand to disable Advanced Power Management

The Advanced Power Management feature is independent of the Standby timer setting. If both Advanced Power Management level and the Standby timer are set, the device will goto the Standby state when the timer times out or the device's Advanced Power Management algorithm indicates that it is time to enter the Standby state.
The IDENTIFY DEVICE response word 83, bit 3 indicates that Advanced Power Management feature is supported if set. Word 86, bit 3 indicates that Advanced Power Management is enabled if set. Word 96, bits 7-0 contain the current Advanced Power Management level if Advanced Power Management is enabled.

11.5.1 Performance Idle Mode

This mode is usually entered immediately after Active mode command processing is complete, instead of conventional idle mode. In Performance Idle mode, all electronic components remain powered and full frequency servo remains operational. This provides instantaneous response to the next command. The duration of this mode is intelligently managed as described below.

11.5.2 Active Idle Mode

In this mode, power consumption is 45-55% less than that of Performance Idle mode. Additional electronics are powered off, and the head is parked near the mid-diameter without servo control. Recovery time to Active mode is about 10ms.

11.5.3 Low Power Idle Mode

Power consumption is 55%-65% less than that of Performance Idle mode. The heads are unloaded on the ramp, however the spindle is still rotated at the full speed. Recovery time to Active mode is about 300ms.

11.5.4 Transition Time

The transition time is dynamically managed by users recent access pattern, instead of fixed times. The ABLE-3 algorithm monitors the interval between commands. The algorithm supposes that next command will come with the same command interval distribution as the previous access pattern. The algorithm calculates the expected average saving energy and response delay for next command in several transition time case based on this assumption. And it selects the most effective transition time with the condition that the calculated response delay is shorter than the value calculated from the specified level by SET FEATURE ENABLE ADAPTIVE POWER MANAGEMENT command.
The optimal time to enter Active Idle mode is variable depending on the users' recent behavior. It is not possible to achieve the same level of Power savings with a fixed entry time into Performance Idle because every users data and access pattern is different. The optimum entry time changes over time.
The same algorithm works for entering into Low Power Idle mode and Standby mode, which consumes less power but need more recovery time switching from this mode to Active mode.

11.6 S.M.A.R.T Function

The intent of Self-Monitoring, Analysis and Reporting Technology (S.M.A.R.T.) is to protect user data and prevent unscheduled system downtime that may be caused by predicable degradation and/or fault of the drive. By monitoring and storing critical performance and calibration parameters, the drive employs sophisticated data analysis algorithms to predict the likelihood of near-term degradation or fault condition, the host system can warn the user of impending risk of data loss and advise the use of appropriate action.

Since S.M.A.R.T. utilizes the internal resource of the drive, there may be some small overhead associated with its operation. However, special care has been taken in the design of S.M.A.R.T. algorithm to minimize the impact to host system performance. To further ensure minimal impact to the user, the drives are shipped from the manufacturer's factory with the S.M.A.R.T. feature disabled.

11.6.1 Attribute values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. Higher attribute values indicate that the analysis algorithms being used by the drive are predicting a lower probability of a degrading or fault condition existing. Accordingly, lower attribute values indicate that the analysis algorithms being used by the drive are predicting higher probabilities of a degrading or fault condition existing. There is no implied linear reliability relationship corresponding to the numerical relationship between different attribute values for any particular attribute.

11.6.2 Attribute thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or faulty condition. The numerical value of the attribute thresholds are determined by the device manufacturer through design and reliability testing and analysis. Each attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and can not be modified in the field. The valid range for attribute threshold is from 1 through 253 decimal.

11.6.3 Threshold exceeded condition

If one or more attribute value are less than or equal to their corresponding attribute thresholds, then the device reliability status is negative, indicating an impending degrading or faulty condition.

11.6.4 S.M.A.R.T. Commands

The S.M.A.R.T. commands provide access to attribute values, attribute thresholds and other logging and reporting information.

11.6.5 S.M.A.R.T. Operation with Power Management modes

The drive saves attribute values automatically on head unload timing except the emergency unload, even if the attribute auto save feature is not enabled. The head unload is done not only by Standby, Standby Immediate, or Sleep command or Hard Reset, but also by the automatic power saving functions like ABLE-3 or Standby timer.

11.7 Seek Overlap

The drive provide accurate seek time measurement method. The SEEK command is usually used to measure the device seek time by accumulating execution time for a number of SEEK commands. With typical implementation of the SEEK command, this measurement must including the device and host command overhead. To eliminate this overhead, overlap the SEEK command as described below.

The first SEEK command completes before the actual seek operation is over. Then device can receive the next SEEK command from the host but actual seek operation for the next SEEK command starts right after the actual seek operation for the first SEEK command is completed. In other words, the execution of two SEEK commands overlaps excluding the actual seek operation. With this overlap, total elapsed time for a number of SEEK commands is the total accumulated time for the actual seek operation plus one pre and post overhead. When the number of seeks is large, just this one overhead can be ignored.

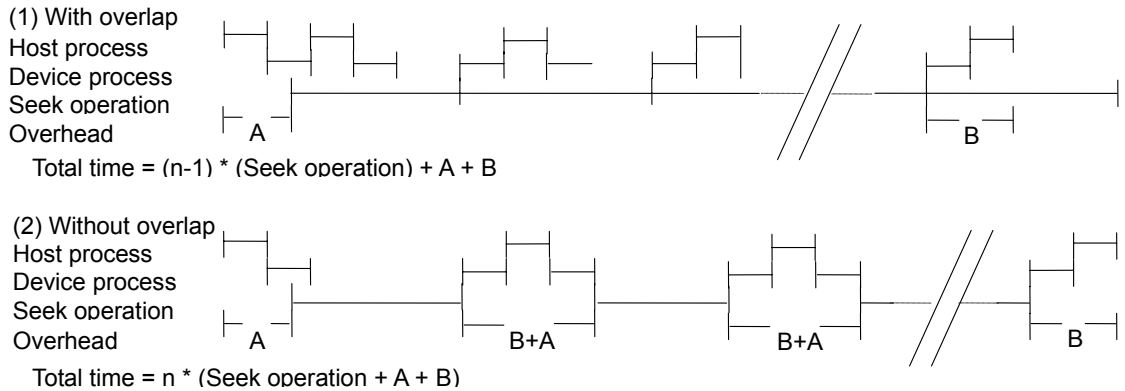


Figure 19 Seek Overlap

11.8 Write Cache Function

Write cache is a performance enhancement whereby the device reports completion of the write command (WRITE SECTORS, WRITE MULTIPLE, WRITE SECTORS WITHOUT ERASE, WRITE MULTIPLE WITHOUT ERASE, WRITE DMA, WRITE VERIFY) to the host as soon as the device has received all of the data into its buffer. The device assumes responsibility to write the data subsequently onto the disk.

While writing data after completed acknowledgment of a write command, soft reset or hard reset does not affect its operation. But power off terminates writing operation immediately and unwritten data are to be lost.

FLUSH CACHE, SOFT RESET, STANDBY, STANDBY IMMEDIATE and SLEEP are executed after the completion of writing to disk media on enabling write cache function. So the host system can confirm the completion of write cache operation by issuing FLUSH CACHE command, SOFT RESET, STANDBY command, STANDBY IMMEDIATE command and SLEEP command, and then, by confirming its completion.

The retry bit of WRITE SECTORS is ignored when write cache is enabled.

11.9 Reassign Function

The Reassign Function is used with read and write commands. The sectors of data for reassignment are prepared as the spare data sector. The number of the spare sectors' entry is 3669. The one entry can register 255 consecutive sectors maximally.
This reassignment information is registered internally, and the information is available right after completing the reassign function. Also the information is used on the next power on reset or hard reset.
If the number of the spare sector reaches 0, the reassign function will be disabled automatically.
The spare tracks for reassignment are located at regular interval. As a result of reassignment, the physical location of logically sequenced sectors will be dispersed.

11.9.1 Auto Reassign Function

The sectors that show some errors may be reallocated automatically when specific conditions are met. The spare sectors for reallocation are located at reserved area. The conditions for auto-reallocation are described below.

Non-recovered write errors

When a write operation can not be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation fails.
If the number of available spare sectors reaches 16 sectors, the write cache function will be disabled automatically.
If the command is without retry and the write cache function is disabled, the auto reassign function is not invoked.

Non-recovered read errors

When a read operation fails after defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

Recovered read errors

When a read operation for a sector failed once then recovered at the specific ERP step, this sector of data is reallocated automatically. A media verification sequence may be run prior to the relocation according to the pre-defined conditions.

11.10 Command Descriptions

11.10.1 Check Power Mode (98h/E5h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	0	V

Figure 20 Check Power Mode Command

The CHECK POWER MODE command allows the host to determine the current power mode of the device.

Input Parameters From The Device

Sector Count The power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the device is not in Standby or Sleep mode. Otherwise, the Sector Count Register will be set to 0.

11.10.2 Execute Device Diagnostic (90h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	-	-	-	-	-
Command	1	0	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	V	V	V	V	V	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	0	0

Figure 21 Execute Device Diagnostic command

The Execute Device Diagnostic command performs the internal diagnostic tests implemented by the device.

The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code.

11.10.3 Flush Cache (E7h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 22 Flush Cache Command

This command causes the device to complete writing data from its cache.

The device returns a status, RDY=1 and DSC=1 (50h), after following sequence.

- Data in the write cache buffer is written to disk media.
- Return a successfully completion.

11.10.4 Format Track (50h) (Vendor Specific)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	L	1	D	H	H	H	H
Command	0	1	0	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	-	-	-	-	H	H	H	H
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 23 Format Track (50h) Command

The Format Track command formats a single logical track on the device. Each good sector of data on the track will be initialized to zero with write operation. At this time, whether the sector of data is initialized correctly is not verified with read operation. Any data previously stored on the track will be lost.

In LBA mode, this command formats a single logical track including the specified LBA.

Output Parameters To The Device

Sector Number	In LBA mode, this register specifies LBA address bits 0 - 7 to be formatted. (L=1) The cylinder number of the track to be formatted. (L=0)
Cylinder High/Low	In LBA mode, this register specifies LBA address bits 8 - 15 (Low), 16 - 23 (High) to be formatted. (L=1)

H	The head number of the track to be formatted. (L=0) In LBA mode, this register specifies LBA address bits 24 - 27 to be formatted. (L=1)
	Input Parameters From The Device
Sector Number	In LBA mode, this register specifies current LBA address bits 0-7. (L=1)
Cylinder High/Low	In LBA mode, this register specifies current LBA address bits 8 - 15 (Low), 16 - 23 (High)
H	In LBA mode, this register specifies current LBA address bits 24 - 27 . (L=1)
Error	The Error Register. An Abort error (ABT=1) will be returned under the following conditions: ・The descriptor value does not match the certain value. (except 00h)

11.10.5 Format Unit (F7h) (Vendor Specific)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 24 Format Unit (F7h)

The Format Unit command initializes all user data sectors after merging reassigned sector location into the defect information of the device and clearing the reassign information. Both new reassign information and new defect information are available right after this command completion, and are also used on next power on reset or hard reset. All previous information are erased from the device by this command.

Note that the Format Unit command initializes from LBA 0 to MAX LBA. Since the command does not perform Auto reassign (See 11.8.1 Auto Reassign Function for detail.) for non-recovered write error, the device may post an ID NOT FOUND ERROR if the device encountered non-recovered write error during the Format Unit command.

The Security Erase Prepare command should be completed immediately prior to the Format Unit command. If the device receives a Format Unit command without a prior Security Erase Prepare command the device aborts the Format Unit command. If Feature register is NOT 11h, the device returns Abort error to the host. This command does not request to data transfer.

Output Parameters To The Device

Feature 11H Merge reassigned location into the defect information.

11.10.6 Identify Device (ECh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	0	V

Figure 25 Identify Device (ECh)

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information in Note 1: See Table 34 Model Name
Table 31 Identify Device Data Structure.

Word Address	Default Value	Total Bytes	Data Field Type Information
0	045Ah	2	Drive Classification
1	Note.1	2	Default number of cylinders
2	0000h	2	Reserved
3	0010h	2	Default number of heads
6	003Fh	2	Default number of sectors per track
7-9	0000h	6	Reserved
10-19	XXXX	20	Serial number in ASCII (Right justified)
20	0003h	4	Don't care
21	0155h	2	Don't care
22	00xxh	2	# of ECC bytes as currently selected via the Set Features Command
23-26	XXXXh	8	Vendor specific Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	Note.3	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	8020h	2	Maximum number of sectors on Read/Write Multiple command
49	0F00h	2	Capabilities
50	4000h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsoleted
53	0007h	2	Translation parameters are valid
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)

59	01XXh	2	Multiple sector setting
60-61	Note.1	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0X07h	2	Multiword DMA Transfer Capability
64	0003h	2	Flow Control PIO Transfer modes supported
65	0078h	2	Minimum Multiword DMA Transfer Cycle Time
66	0078h	2	Manufacturer's Recommended Multiword DMA Transfer Cycle Time
67	0078h	2	Minimum PIO Transfer Cycle Time without Flow Control
68	0078h	2	Minimum PIO Transfer Cycle Time with IORDY Flow Control
69-79	0000h	2	Reserved
80	001Eh	2	Major Version Number
81	0012h	2	Minor Version Number
82	7069h	2	Command Set supported
83	5008h	2	Command Set supported
84	6000h	2	Command Set/Feature supported Extent ion
85	7048h	2	Command Set/Feature Enabled
86	1008h	2	Command Set/Feature Enabled
87	6000h	2	Command Set/Feature Enabled
88	0007h	2	Ultra DMA Transfer Capability
89-90	0000h	4	Reserved
91	40XXh	2	Current Advanced Power Management Level
92-255	xxxxh		Don’t care

Note 1: See Table 34 Model Name

Table 31 Identify Device Data Structure

Word 0: General Configuration

Bit		
15	0	1 = ATAPI device, 0 = ATA device
14	0	1 = format speed tolerance gap required
13	0	1 = track offset option available
12	0	1 = data strobe offset option available
11	0	1 = rotational speed tolerance > 0.5%
10	1	1 = disk transfer rate > 10 Mbps
9	0	1 = disk transfer rate > 5 Mbps but <= 10 Mbps
8	0	1 = disk transfer rate <= 5 Mbps
7	0	1 = removable cartridge device
6	1	1 = fixed device
5	0	1 = spindle motor control option implemented
4	0	1 = head switch time > 15usec
3	1	1 = not MFM encoded
2	0	1 = Identify data incomplete
1	1	1 = hard sectored
0	0	reserved

Table 32 Identify Device Word 0

Word 1: Default Number of Cylinders

Word 3: Default Number of Heads

Word 6: Default Number of Sectors per Track

The default logical parameter of the device is;

	3K8-10	3K8-8	3K8-6	3K8-4
Number of Heads	16	16	16	16
Sectors per Track	63	63	63	63
Number of Cylinders	19377	15501	11905	7936
Number of Sectors	19532016	15625008	12000556	799488

Table 33 Default Logical Parameters of the device

Word 9 - 10: Device Serial Number

This field contains the serial number of the device. The contents of this field are right justified and padded with ASCII spaces (20h).

Word 23 - 26: Firmware Revision

This field contains the revision of the firmware in ASCII

Word 27 - 46: Model Number

This field contains the model number of the device. The contents of this field are left justified and padded with ASCII spaces (20h).

Type	Model Name
3K8-8	HMS361008M5CE00
3K8-6	HMS361006M5CE00
3K8-4	HMS361004M5CE00

Table 34 Model Name

Word 49: Capabilities

Bit		
15-14	0	Reserved
13	0	0 = Standby timer value is vendor specific
12	0	Reserved
11	1	1 = IORDY supported
10	1	1 = IORDY can be disabled
9	1	1 = LBA mode supported
8	1	1 = DMA transfer supported
7 - 0	0	Reserved

Word 50: Capabilities

Bit		
15	0	0 = As specified by ATA reference
14	1	1 = As specified by ATA reference
13-1	0	Reserved
0	0	1 = the device has minimum standby timer value that is device specific

Word 51: PIO data transfer mode number

Bit	
15-8	PIO data transfer mode number
7 - 0	Reserved

Word 53:Translatation parameters are valid

Bit		
15-3	0	Reserved
2	1	1 = the fields reported in Word 88 are valid
1	1	1 = the fields reported in Words 64-70 are valid
0	1	1 = the fields reported in Words 54-58 are valid

Word 59: Multiple Sector Setting

Bit		
15-9	0	Reserved
8	1	1 = Multiple sector setting is valid
7 - 0	XX	XXh =Current setting for number of sectors transferred per interrupt on R/W multiple command

Word 63: Multiword DMA Transfer Capability

Bit		
15-11	0	Reserved
10	X	1 = Multiword DMA mode 2 is selected
9	X	1 = Multiword DMA mode 1 is selected
8	X	1 = Multiword DMA mode 0 is selected
7 - 3	0	Reserved
2	1	1 = Multiword DMA mode 2 is supported
1	1	1 = Multiword DMA mode 1 is supported
0	1	1 = Multiword DMA mode 0 is supported

Word 64: Flow Control PIO Transfer Modes Supported

Bit		
15-2	0	Reserved
1	1	1 = the device supports PIO mode 4
0	1	1 = the device supports PIO mode 3

Word 80: Major Version Number

Bit		
15-5	0	Reserved
4	1	1 = the device supports ATA/ATAPI-4
3	1	1 = the device supports ATA-3
2	1	1 = the device supports ATA-2
1	1	1 = the device supports ATA-1
0	0	Reserved

Word 82: Command Sets Supported

Bit		
15	0	Reserved
14	1	1 = NOP command supported
13	1	1 = Read Buffer command supported
12	1	1 = Write Buffer command supported
11	0	Reserved
10	0	1 = Host Protected Area Feature Set supported
9	0	1 = Device Reset Command supported
8	0	1 = Service interrupt supported
7	0	1 = release interrupt supported
6	1	1 = Look-Ahead supported
5	1	1 = write cache supported
4	0	1 = PACKET command Feature set supported
3	1	1 = Power management Feature set supported
2	0	1 = Removable Media Feature set supported
1	0	1 = Security Feature set supported
0	1	1 = S.M.A.R.T. Feature set supported

Word 83: Command Sets supported

Bit		
15	0	0 = As specified by ATA reference
14	1	1 = As specified by ATA reference
13-5	0	Reserved
4	0	1 =Removable Media status Notification feature set supported
3	1	1 = Advanced Power Management feature set supported
2	0	1 = CFA feature set supported
1	0	1 = Read/Write DMA Queued supported
0	0	1 = DOWNLOAD MICROCODE command supported

Word 84: Command Sets Supported Extension

Bit		
15	0	0 = As specified by ATA reference
14	1	1 = As specified by ATA reference
13	1	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported
12-0	0	0 = Reserved

Word 85: Command Set/Feature Enabled

Bit		
15	0	Reserved
14	1	1 = NOP command supported
13	1	1 = Read Buffer Command supported
12	1	1 = Write Buffer Command supported
11	0	Reserved
10	0	1 = Host Protected Area Feature set supported
9	0	1 = Device Reset command supported
8	0	1 = Service interrupt enabled
7	0	1 = release interrupt enabled
6	X	1 = Look-Ahead enabled
5	X	1 = Write Cache enabled
4	0	1 = PACKET command feature set supported
3	1	1 = Power Management feature set supported
2	0	1 = Removable Media feature set supported
1	0	1 = Security Mode feature set supported
0	X	1 = S.M.A.R.T. feature set enabled

Word 86: Command Set/Feature Enabled

Bit		
15-13	0	Reserved
12	1	1 = FLUSH CACHE command supported
11-5	0	Reserved
4	0	1 = Removable Media Status Notification feature set enabled
3	X	1 = Advanced Power Management feature set enabled
2	0	1 = CFA feature set supported
1	0	1 = Read/Write DMA Queued command supported
0	0	1 = DOWNLOAD MICROCODE command supported

Word 87: Command Set/Feature default

Bit		
15	0	0 = As specified by ATA reference
14	1	1 = As specified by ATA reference
13	1	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported
12-0	0	0 = Reserved

Word 88: Ultra DMA Transfer Capability

Bit		
15-11	0	Reserved
10	X	1 = Ultra DMA mode 2 is selected
9	X	1 = Ultra DMA mode 1 is selected
8	X	1 = Ultra DMA mode 0 is selected
7-3	0	Reserved
2	1	1 = Ultra DMA mode 2 and below are supported
1	1	1 = Ultra DMA mode 1 and below are supported
0	1	1 = Ultra DMA mode 0 and below are supported

Word 91: Current Advanced Power Management Level

Bit		
15-8	40h	For compatibility
7-0	XXh	Current Advanced Power Management level set by Set Features Command (01h – FEh)

11.10.7 Idle (E3h/97h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 26 Idle Command (E3h/97h)

The Idle command causes the device to enter Idle mode immediately, and set auto power down timeout parameter (standby timer). Then the timer starts counting down.
When the Idle mode is entered, the device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.
During Idle mode, the device is spinning and ready to respond to host command immediately.

Output Parameters To The Device

Sector Count Timeout Parameter. If zero, the timeout interval(Standby Timer) is NOT disabled, but the timeout interval is set for 109 minutes automatically. If other than zero, the timeout interval is set for (Timeout Parameter x5) seconds.
The device will enter Standby mode automatically if the timeout interval expires with no device access from the host. The timeout interval will be reinitialized if there is a device access before the timeout interval expires.

11.10.8 Idle Immediate (E1h/95h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 27 Idle Immediate Command (E1h/95h)

The Idle Immediate command causes the device to enter Idle mode. The device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed. During Idle mode, the device is spinning and ready to respond to host commands immediately.
The Idle Immediate command will not affect the auto power down timeout parameter.

11.10.9 Idle Immediate with Unload (E1h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	1	0	0	0	1	0	0
Sector Count	0	0	0	0	0	0	0	0
Sector Number	0	1	0	0	1	1	0	0
Cylinder Low	0	1	0	0	1	1	1	0
Cylinder High	0	1	0	1	0	1	0	1
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	1	1	0	0	0	1	0	0
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 28 Idle Immediate Command with Unload (E1h)

The Idle Immediate command with Unload option causes the device to immediately unload the heads. Although the time to complete the unload operation is vendor specific, the typical value is within 500msec of receiving the command. The device will stay at Low Power Idle mode, will not go into Standby mode and will not load the heads until receiving a new command.

11.10.10 Initialize Device Parameters (91h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	H	H	H	H
Command	1	0	0	1	0	0	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	-	-	0	0	V

Figure 29 Initialize Device Parameters Command (91h)

The Initialize Device Parameters command enables the host to set the number of sectors per track and the number of heads minus 1 per cylinder. The words 54-58 in Identify Device Information reflect these parameters. The parameters remain in effect until the following events;

- Another Initialize Device Parameters command is received
- The device is powered off
- Hard reset occurs
- Soft reset occurs and the Set Features option of CCh is set.

Output Parameters To The Device

Sector Count	The number of sectors per track. 0 does not mean there are 256 sectors per track, but there is no sector per track.
H	The number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

11.10.11 Read Buffer (E4h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	0	V

Figure 30 Read Buffer Command (E4h)

The Read Buffer command transfers a sector of data from the device's buffer to the host.
The sector transferred will be the same part of the buffer written to by the last Write Buffer command.
The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

11.10.12 Read DMA (C8h/C9h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	-	1	D	H	H	H	H
Command	1	1	0	0	1	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	-	-	-	-	H	H	H	H
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 31 Read DMA Command (C8h/C9h)

The Read DMA command reads one or more sectors of data from disk media, and then transfers the data from the device to the host. The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only on interrupt per command to indicate that data transfer has terminated and status is available. If an un-correctable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count — The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number — The sector number of the first sector to be transferred. (L=0)
In LBA mode, this register specifies LBA address bits 0 - 7 to be transferred.

	(L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register specifies LBA address bits 8 - 15 (Low) 16 - 23 (High) to be transferred. (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register specifies LBA bits 24-27 to be transferred. (L=1)
R	The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.10.13 Read Long (22h/23h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	0	0	0	0	0	0	0	1
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	-	-	-	-	H	H	H	H
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 32 Read Long Command (22h/23h)

The Read Long command reads the designated one sector of data and the ECC bytes from the disk media, and then transfers the data and ECC bytes from the data and ECC bytes from the device to the host.

After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes is 4 or 51 according to the setting of Set Feature option. The default setting is 4 bytes of ECC data.

The command makes a single attempt to read the data and does not check the data using ECC. Whatever is read is returned to the host.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register specifies LBA address bits 0 - 7 to be transferred. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register specifies LBA address bits 8 - 15 (Low) 16 - 23 (High) to be transferred. (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register specifies LBA bits 24-27 (L=1)
R	The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

It should be noted that the device internally uses 51 bytes of ECC data on all data written or read from the disk. The 4 bytes mode of operation is provided via emulation. It is recommended that for testing the effectiveness and integrity of the device ECC functions that the 51 byte ECC mode should be used.

11.10.14 Read Multiple (C4h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	-	-	-	-	H	H	H	H
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 33 Read Multiple Command (C4h)

The Read Multiple command reads one or more sectors of data from disk media, and then transfers the data from the device to the host. The execution of the command is identical to the Read Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of each sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register specifies LBA address bits 8 - 15 (Low) 16 - 23 (High) to be transferred. (L=1)

H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register specifies LBA bits 24-27 (L=1)
	Input Parameters From The Device
Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.10.15 Read Sectors (20h/21h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	-	-	-	-	H	H	H	H
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 34 Read Sectors Command (20h/21h)

The Read Sectors command reads one or more sectors of data from disk media, and then transfers the data from the device to the host. If an un-correctable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0)

	In LBA mode, this register contains LBA bits 24 - 27. (L=1)
R	The retry bit. If set to one, then retries are disabled.
	Input Parameters From The Device
Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.10.16 Read Verify Sectors (40h/41h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	L	1	D	H	H	H	H
Command	0	0	1	0	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	-	-	-	-	H	H	H	H
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	V	0	V	0	V	0	V

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 35 Read Verify Sectors Command (40h/41h)

The Read Verify Sectors verifies one or more sectors on the device. No data is transferred to the host. The difference of Read Sectors command and Read Verify Sectors command is whether the data is transferred to the host or not. If an un-correctable error occurs, the read verify will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be verified. If zero is specified, then 256 sectors will be verified.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 - 27. (L=1)
R	The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not verified. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.10.17 Recalibrate (1Xh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	0	0	0	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	V	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 36 Recalibrate Command (1Xh)

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0. If the device can not reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

11.10.18 Security Erase Prepare (F3h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	0	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 37 Security Erase Prepare (F3h)

The Security Erase Prepare Command must be issued immediately before the Format Unit to prevent accidental erasure of the device. This command does not request to transfer data.

11.10.19 Seek (7Xh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	L	1	D	H	H	H	H
Command	0	1	1	1	-	-	-	-

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	-	-	-	-	H	H	H	H
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 38 Seek Command (7Xh)

The Seek command initiates a seek to the designated track and selects designated head.

Output Parameters To The Device

Sector Number — In LBA mode, this register specifies LBA address bits 0 - 7 for seek. (L=1)

Cylinder High/Low — The cylinder number of the seek.
In LBA mode, this register specifies LBA address bits 8 - 15 (Low), 16 - 23 (High) for seek. (L=1)

H — The head number of the seek.
In LBA mode, this register specifies LBA address bits 24 - 27 for seek. (L=1)

Input Parameters From The Device

Sector Number — In LBA mode, this register contains current LBA bits 0 - 7. (L=1)

Cylinder High/Low — In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H	In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.10.20 Sense Condition (F0h:Vendor Unique)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	0	0	0	0	0	0	0	1
Sector Count	-	-	-	-	-	-	-	-
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	D	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	V	0	V	-	-	0	V

Figure 39 Sense Condition Command (F0h)

The Sense Condition command is used to sense temperature in a device. This command is executable without spinning up.

Output Parameters To The Device

Feature

The Feature register must be set to 01h. All other value are rejected with setting ABORT bit in status register.

Input Parameters From The Device

Sector Count

The Sector Count register contains result value.

Value	Description
00h	Temperature is equal to or lower than -20 degC
01h-FEh	Temperature is (Value / 2 - 20) deg C
FFh	Temperature is higher than 107 degC

11.10.21 Set E.S.P. Threshold (8Ch) (Vendor Unique)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	1	1	0	1	1	1	0	1
Sector Count	-	-	-	-	-	-	-	-
Sector Number	0	0	0	0	0	0	V	V
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	0	0	0	1	1	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	V	0	-	-	0	0	V

Figure 40 Set E.S.P. Threshold Command (8Ch) (Vendor Unique)

The Set E.S.P. Threshold command allows customers to change threshold level of ESP feature. This command is supported by E.S.P. models only. ABT will be set to 1 in the Error Register if the Sector Number contains any undefined values. If feature register value is not 0DDh, the behavior of the device is undetermined.

Sector Number	Threshold
00h	Disable ESP
01h	Low Sensitivity: This mode gives minimum risk of performance degradation due to head unload operation by ESP feature. The device will detect drop event around 370 mm drop. The device attempts to resume from drop event at minimum wait time after setting from drop event.

02h	Middle Sensitivity mode: This mode is shipping default of the device. The device will detect drop event around 180 mm drop.
03h	High Sensitivity: This mode gives maximum protection against drop events. The device will detect drop events around 130 mm. However, the device may suspend its medium access operation due to false drop detection.

Table 35 Supported E.S.P. Thresholds

11.10.22 Set Features (EFh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	Note. 1							
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	1	1	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	V	0	-	-	0	0	V

Figure 41 Set Features Command (EFh)

The Set Features command establishes the following parameters which affect the execution of certain features as shown in below table. ABT will be set to 1 in the Error Register if the Feature contains any undefined values.

Feature	Operation
02h	Enable Write Cache
03h	Used for Set Transfer Mode command
05h	Set Advanced Power Management Mode
44h	Product specific ECC bytes (51 bytes) apply on Read/Write Long commands
55h	Disable Read Look Ahead
66h	Disable Power on Reset (POR) establishment of defaults at Soft Reset

69h	NOP n Accepted for backward compatibility
82h	Disable Write Cache
85h	Disable Advanced Power Management
96h	NOP n Accepted for backward compatibility
97h	Accepted for backward compatibility. Use of this feature is not recommended
9Ah	NOP n Accepted for backward compatibility
AAh	Enable Read Look Ahead
BBh	4 bytes of ECC apply on Read/Write Long commands
CCh	Enable Power on Rest (POR) establishment of defaults at Soft Reset

Table 36 Supported Features

Features 82h, AAh and BBh are the default features for the device, thus the host does not have to issue this command with these features unless it is necessary for compatibility reasons.
Features 66h and CCh can be used to enable and disable whether the Power On Reset (POR) defaults will be set when a soft reset occurs. The default setting is to revert to the POR defaults when a soft reset occurs.
Feature 05h is used for advanced power management. The Sector Count Register specifies the advanced power management level as below. The advanced power management level at power on reset is 60h.

- 80h – FEh : Up to Low Power Idle mode
- 01h – 7Fh : Up to Standby mode
- 00h, FFh : Reserved

Feature 85h is used to disable advanced power management. This results in the same effect as the host uses features 05h with Sector Count Register FEh.

11.10.23 Set Multiple (C6h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	0	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	0	V

Figure 42 Set Multiple Command (C6h)

The Set Multiple command enables the device to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt. The default block size after power up, or hard reset is 0, and Read Multiple and Write Multiple commands are disabled. If an invalid block size is specified, and ABT bit in the Error Register to indicate the command is aborted. Read Multiple and Write Multiple commands will be disabled.

Output Parameters To The Device

Sector Count The block size to be used for Read Multiple and Write Multiple commands. Valid block sizes can be selected from 0, 1, 2, 4, 8, 16 or 32. If 0 is specified, then Read Multiple and Write Multiple commands are disabled.

11.10.24 Sleep (E6h/99h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	1	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 43 Sleep Command (E6h/99h)

The Sleep command causes the device to enter the Sleep Mode Immediately. When this command is issued, the device confirms the completion of the cached write commands before it asserts INTRQ. Then the device is spun down. If the device is already spun down, the spin down sequence is not executed. It is not required to use and software reset or hardware reset to recover from Sleep mode, but simply issue a command to the device.

11.10.25 S.M.A.R.T. Function Set (B0h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	V	V	V	V	V	V	V	V
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	0	1	0	0	1	1	1	1
Cylinder High	1	1	0	0	0	0	1	0
Device / Head	1	0	1	D	-	-	-	-
Command	1	0	1	1	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	-	V

Figure 44 S.M.A.R.T. Function Set Command (B0h)

The S.M.A.R.T. Function Set Command provides access to Attribute Values, Attribute Thresholds and other low level subcommands that can be used for logging and reporting purpose and to accommodate special user needs. The S.M.A.R.T. Function Set Command has several separate subcommands which are selectable via the device's Feature Register when the S.M.A.R.T. Function Set command is issued by the host.

In order to select a subcommand the host must write the subcommand code to the device's Feature Register before issuing the S.M.A.R.T. Function Set command. The subcommand and their respective codes are listed below.

	code	Description
S.M.A.R.T. Read Attribute Values	D0h	This sub-command returns the device's Attribute Value to the host. The total size of Attribute Values is 512 bytes.
S.M.A.R.T. Read Attribute Threshold	D1h	This sub-command returns the device's Attribute Threshold Value to the host. The total size of Attribute Threshold Values is 512 bytes.
S.M.A.R.T. Enable/Disable Attribute Autosave	D2h	This sub-command enables/disables the attribute autosave feature of the device. A value of 00h in Sector Count Register while this sub-command is being issued causes Attribute Autosave feature disabled. A value of F1h in Sector Count Register while this sub-command is being issued causes Attribute Autosave feature enabled. Any other Sector Count Register value will not change the current state of Autosave feature. However, regardless of the state of autsave feature, the device may perform saving S.M.A.R.T. attributes when it makes transition to Standby mode or Sleep mode. The S.M.A.R.T. disable operations sub-command also disables the autosave feature along with device's S.M.A.R.T. operation.

<table>
<tr>
<td>S.M.A.R.T. Execute Off-line Immediate</td>
<td>D4h</td>
<td>This sub-command causes the device to immediately initiate the set of activities that collect Attribute data in an off-line mode or execute a self-test routine in either captive or off-line mode.
The contents of Sector Number Register direct the device which operation to be executed.
<table>
<tr><td>Sector Number</td><td>Operation to be executed</td></tr>
<tr><td>0h</td><td>Execute S.M.A.R.T. off-line data collection immediately</td></tr>
<tr><td>1h</td><td>Execute S.M.A.R.T. Short self-test immediately in off-line mode</td></tr>
<tr><td>2h</td><td>Execute S.M.A.R.T. Extended self-test immediately in off-line mode</td></tr>
<tr><td>7Fh</td><td>Abort off-line mode self-test.</td></tr>
<tr><td>81h</td><td>Execute S.M.A.R.T. Short self-test immediately in captive mode</td></tr>
<tr><td>82h</td><td>Execute S.M.A.R.T. Extended self-test immediately in captive mode</td></tr>
</table>
Off-line mode: The device posts command completion before executing the specific test. During execution of the operation, the device will not post BSY. If the execution of the operation is interrupted by a new command from the host, the device will abort or suspend the operation and will service the new command as soon as possible. After servicing interrupting command, the device will resume the operation or not start the operation depending on the interrupting command
Captive mode: The device executes the operation after receipt of the command. At the end of operation, the device reports the execution result in self-test execution status byte and ATA registers as below.
Status ERR bit set when self-test has failed
Error ABT bit set when self-test has failed
Cylinder Low F4h when self-test has failed
Cylinder High 2Ch when self-test has failed</td>
</tr>
</table>

S.M.A.R.T. Enable Operations	D8h	This sub-command enables access to all S.M.A.R.T. capabilities within the device. The state of S.M.A.R.T. will be preserved by the device across power cycle. Once enabled, the receipt of subsequent S.M.A.R.T. Enable Operations sub-command will not affect any of the Attribute Values.
S.M.A.R.T. Disable Operations	D9h	This sub-command disables all S.M.A.R.T. capabilities within the device. The state of S.M.A.R.T. will be preserved by the device across power cycle.
S.M.A.R.T. Return Status	DAh	This sub-command is used to communicate the reliability status of the device to the host's request. If the device does not detect a Threshold Exceeded Condition but involving attributes are advisory, the device loads 4Fh into the Cylinder Low Register and C2h into the Cylinder High Register respectively. If the device detects a Threshold Exceeded Condition for prefailure attributes, the device loads F4h into the Cylinder Low Register and 2Ch into the Cylinder High Register respectively.

Table 37 S.M.A.R.T. Subcommands

Device Attribute Data Structure

The following table describes the 512 byte Attribute Value information being accessed by the host using S.M.A.R.T. Read Attribute Values sub-command. All multi-byte fields shown in these data structures follow the ATA/ATAPI-7 specification for byte ordering, namely that the least significant byte occupies the lowest numbered byte address location the field.

Description	Offset	Size (bytes)
Data Structure Revision Number	0	2
1st Device Attribute	2	12
…..		
30th Device Attribute	350	12
Offline data collection status	362	1
Self-test execution status	363	1
Total time in seconds to complete off-line data collection activity	364	2
Current segment pointer	366	1

Off-line data collection capability	367	1
S.M.A.R.T. capability	368	2
S.M.A.R.T. device error logging capability	370	1
Self-test failure check point	371	1
Short self-test completion time in minutes	372	1
Extended self-test completion time in minutes	373	1
Reserved	374	12
Vendor Specific	386	125
Data structure check sum	511	1

Table 38 S.M.A.R.T. Device Attribute Data Structure

Individual Attribute Data Structure

The following table describes the 12 byte each attribute entry in the device attribute data structure.

Description	Offset	Size (bytes)
Attribute ID Number	0	1
Status Flags Bit: Description 15-6: = 0 Reserved 5 - 2: Reserved 1: On-line collection 0: Pre-failure/Advisory	1	2
Attribute Value Value: Description 00h: Invalid value – not to be referred 01h: Minimum value FDh: Maximum value FEh: Value is not valid FFh: Invalid value – not to be referred	3	1
Reserved	4	7
Reserved (00h)	11	1

Table 39 S.M.A.R.T. Individual Attribute Data Structure

Attribute ID Numbers

ID	Description	Pre-failure
0	Indicates this entry in the data structure is not used	
1	Raw Read Error Rate	
3	Spin Up Time	✓
4	Start/Stop Count	
5	Reallocated Sector Count	✓
7	Seek Error Rate	
8	Seek Time	
9	Power On Hours	
10	Spin Retry Count	✓
12	Power Cycle Count	
192	Power Off Retract Count	
193	Load/Unload Cycle Count	
194	Device Temperature	
196	Reallocation Event Count	
197	Current Pending Sector Count	
199	Ultra DMA CRC Error Count	
220	Disk Shift Value	

Table 40 S.M.A.R.T. Attribute ID

11.10.26 Standby (E2h/96h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	1	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 45 Standby Command (E2h/96h)

The Standby command causes the device to enter the Standby Mode immediately, and set auto power down timeout parameter (standby timer). When this command is issued, the device confirms the completion of the cached write commands before it asserts INTRQ. Then the device is spun down, but the interface remains active. If the device is already spun down, the spin down sequence is not executed. During the Standby mode, the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed. The timer starts counting down when the device returns to Idle mode.

Output Parameters To The Device

Sector Count

Timeout Parameter. If zero, the timeout interval(Standby Timer) is NOT disabled, but the timeout interval is set to 109 minutes automatically. If other than zero, the timeout interval is set for (Timeout Parameter x5) seconds.

When the automatic power down sequence is enabled,

The device will enter Standby mode automatically if the timeout interval expires with no device access from the host. The timeout interval will be reinitialized if there is a device access before the timeout interval expires.

11.10.27 Standby Immediate (E0h/94h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	0	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	-	0	0	V

Figure 46 Standby Immediate Command (E0h/94h)

The Standby Immediate command causes the device to enter Standby Mode Immediately. When this command is issued, the device confirms the completion of the cached write commands before asserts INTRQ. Then the device is spun down, but the interface remains active.
If the device is already spun down, the spin down sequence is not executed. During the Standby mode, the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed. The Standby Immediate command will not affect the auto power down timeout parameters.

11.10.28 Write Buffer (E8h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	1	-	1	D	-	-	-	-
Command	1	1	1	0	1	0	0	0

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	-
Sector Number	-	-	-	-	-	-	-	-
Cylinder Low	-	-	-	-	-	-	-	-
Cylinder High	-	-	-	-	-	-	-	-
Device / Head	-	-	-	-	-	-	-	-
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	0	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	-	-	0	0	V

Figure 47 Write Buffer Command (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer of the device. The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within the buffer.

11.10.29 Write DMA (CAh/CBh)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	1	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	-	-	-	-	H	H	H	H
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
V	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 48 Write DMA Command (CAh/CBh)

The Write DMA command transfers one or more sectors of data from the host to the device, and then the data is written to the disk media. The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available. If an un-correctable error occurs when write cache feature is disabled, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0)

	In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 - 27. (L=1)
R	The retry bit. If set to one, then retries are disabled. When write cache is enabled, They are ignored. (Ignoring the retry bit is in violation of ATA-3.)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.10.30 Write Long (32h/33h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	0	0	0	0	0	0	0	1
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	1	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	-	-	-	-	-	-	-	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	-	-	-	-	H	H	H	H
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 49 Write Long Command (32h/33h)

The Write Long command transfers the data and the ECC bytes of the designated one sector from the host to the device, and then the data and the ECC bytes are written to the disk media.
After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to receive the ECC bytes from the host. The data is transferred 16 bits at the time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes is 4 or 51 according to setting of Set Feature option. The default number after power on is 4 bytes.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. The Sector Count must be set to one.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0)

	In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 - 27. (L=1)
R	The retry bit. If set to one, then retries are disabled.
	Input Parameters From The Device
Sector Count	The number of requested sectors not transferred.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

The device internally uses 51 bytes of ECC on all data read or writes. The 4 byte mode of operation is provided via emulation technique. As a consequence of this emulation, it is recommended that 51 byte ECC mode is used for all tests to confirm the operation of device ECC hardware. Unexpected result may occur if such testing is performed using 4 byte mode.

11.10.31 Write Multiple (C5h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	L	1	D	H	H	H	H
Command	1	1	0	0	0	1	0	1

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	-	-	-	-	H	H	H	H
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 50 Write Multiple Command (C5h)

The Write Multiple command transfers one or more sectors from the host to the device, and then the data is written to the disk media. The execution of command is identical to the Write Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H	The head number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.10.32 Write Sectors (30h/31h)

Command Block Output Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Feature	-	-	-	-	-	-	-	-
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	1	L	1	D	H	H	H	H
Command	0	0	1	1	0	0	0	R

Command Block Input Registers								
Register	7	6	5	4	3	2	1	0
Data	-	-	-	-	-	-	-	-
Error	…See Below …							
Sector Count	V	V	V	V	V	V	V	V
Sector Number	V	V	V	V	V	V	V	V
Cylinder Low	V	V	V	V	V	V	V	V
Cylinder High	V	V	V	V	V	V	V	V
Device / Head	-	-	-	-	H	H	H	H
Status	…See Below …							

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	-	0	0	V

Figure 51 Write Sectors Command (30h/31h)

The Write Sectors command transfers one or more sectors from the host to the device, and then the data is written to the disk media. If an un-correctable error occurs when write cache feature is disabled, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count	The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.
Sector Number	The sector number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the first sector to be transferred. (L=0) In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the first sector to be transferred. (L=0)

R	In LBA mode, this register contains LBA bits 24 - 27. (L=1) The retry bit. If set to one, then retries are disabled. But ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-3.)
	Input Parameters From The Device
Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0) In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0)In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

11.11 Error Posting

The following table summarizes the valid status and error value for all supported command set.

V=Valid on this command

	Error Register					Status Register				
COMMAND	**CRC**	**UNC**	**IDNF**	**ABRT**	**AMNF**	**DRDY**	**DWF**	**DSC**	**CORR**	**ERR**
CheckPower Mode				V		V	V	V		V
Execute Device Diagnostic						V		V		V
Flush Cache			V	V	V	V		V		V
Format Track			V	V	V	V	V	V		V
Identify Device				V		V	V	V		V
Idle				V		V	V	V		V
Idle Immediate				V		V	V	V		V
Initialize Device Parameters						V		V		V
Read Buffer				V		V	V	V		V
Read DMA	V	V	V	V	V	V	V	V	V	V
Read Multiple		V	V	V	V	V	V	V		V
Read Long Sector			V	V	V	V	V	V		V
Read Sector(s)		V	V	V	V	V	V	V	V	V
Read Verify Sectors		V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Seek			V	V		V	V	V		V
Sense Condition				V		V	V	V		V
Set Features				V		V	V	V		V
Set Multiple Mode				V		V	V	V		V
Set Sleep Mode				V		V	V	V		V
Standby				V		V	V	V		V
Standby Immediate				V		V	V	V		V
Write Buffer				V		V	V	V		V

Table 41 Error Reporting