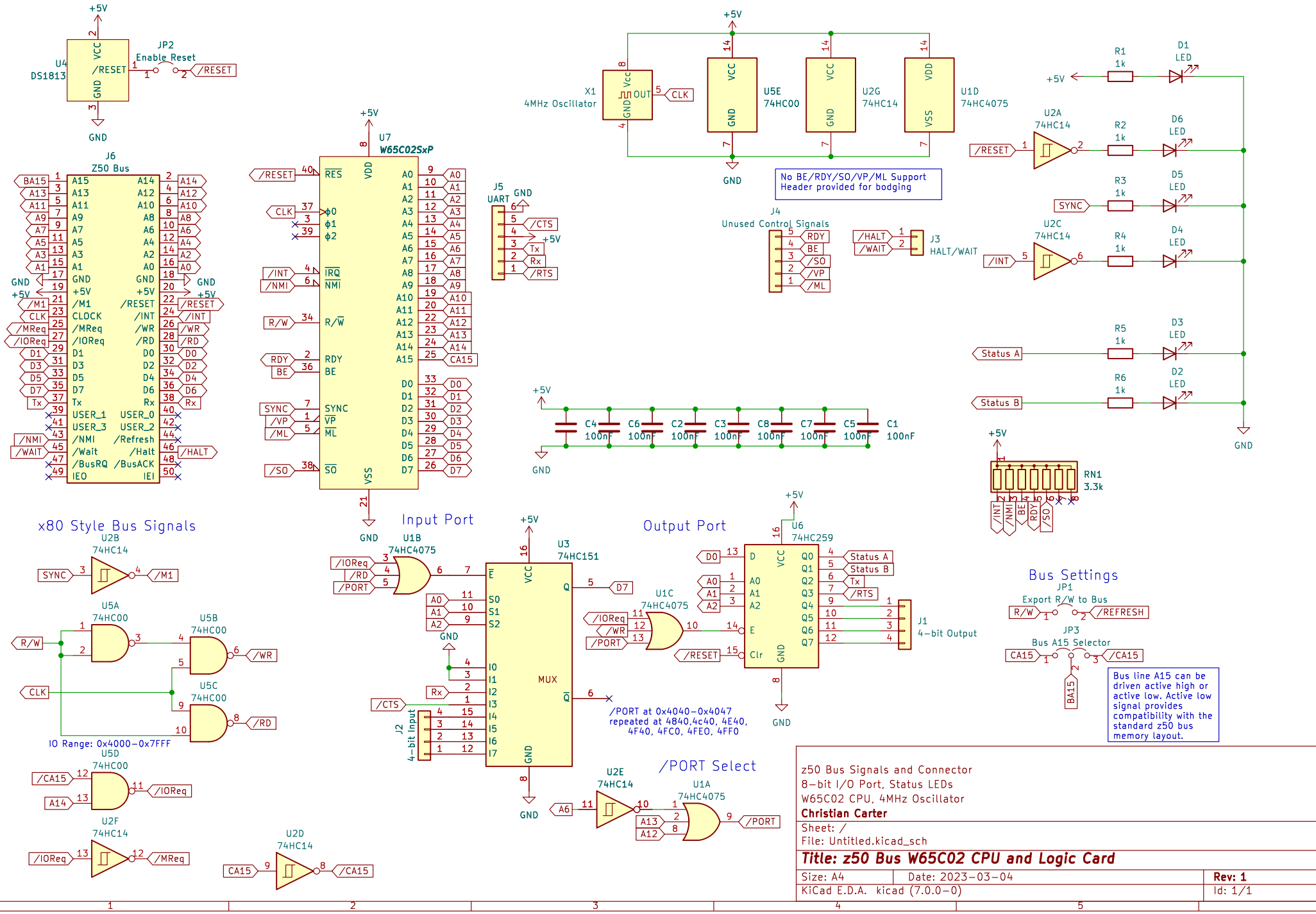
U4
DS1813
JP2
Enable Reset
/RESET
GND
J6
Z50 Bus
U7
W65C02SxP
X1
4MHz Oscillator
U5E
74HC00
U2G
74HC14
U1D
74HC4075
No BE/RDY/SO/VP/ML Support
Header provided for bodging
J5
UART
J4
Unused Control Signals
J3
HALT/WAIT
U2A
74HC14
U2C
74HC14
R1
1k
D1
LED
R2
1k
D6
LED
R3
1k
D5
LED
R4
1k
D4
LED
R5
1k
D3
LED
R6
1k
D2
LED
Status A
Status B
C4
100nF
C6
100nF
C2
100nF
C3
100nF
C8
100nF
C7
100nF
C5
100nF
C1
100nF
RN1
3.3k
x80 Style Bus Signals
U2B
74HC14
U5A
74HC00
U5B
74HC00
U5C
74HC00
U5D
74HC00
U2F
74HC14
IO Range: 0x4000–0x7FFF
U2D
74HC14
Input Port
U1B
74HC4075
U3
74HC151
J2
4-bit Input
Output Port
U6
74HC259
U1C
74HC4075
J1
4-bit Output
/PORT at 0x4040–0x4047
repeated at 4840,4c40, 4E40,
4F40, 4FC0, 4FE0, 4FF0
/PORT Select
U2E
74HC14
U1A
74HC4075
Bus Settings
JP1
Export R/W to Bus
JP3
Bus A15 Selector
Bus line A15 can be
driven active high or
active low. Active low
signal provides
compatibility with the
standard z50 bus
memory layout.
z50 Bus Signals and Connector
8–bit I/O Port, Status LEDs
W65C02 CPU, 4MHz Oscillator
Christian Carter
Sheet: /
File: Untitled.kicad_sch
Title: z50 Bus W65C02 CPU and Logic Card
Size: A4
Date: 2023–03–04
Rev: 1
KiCad E.D.A. kicad (7.0.0–0)
Id: 1/1