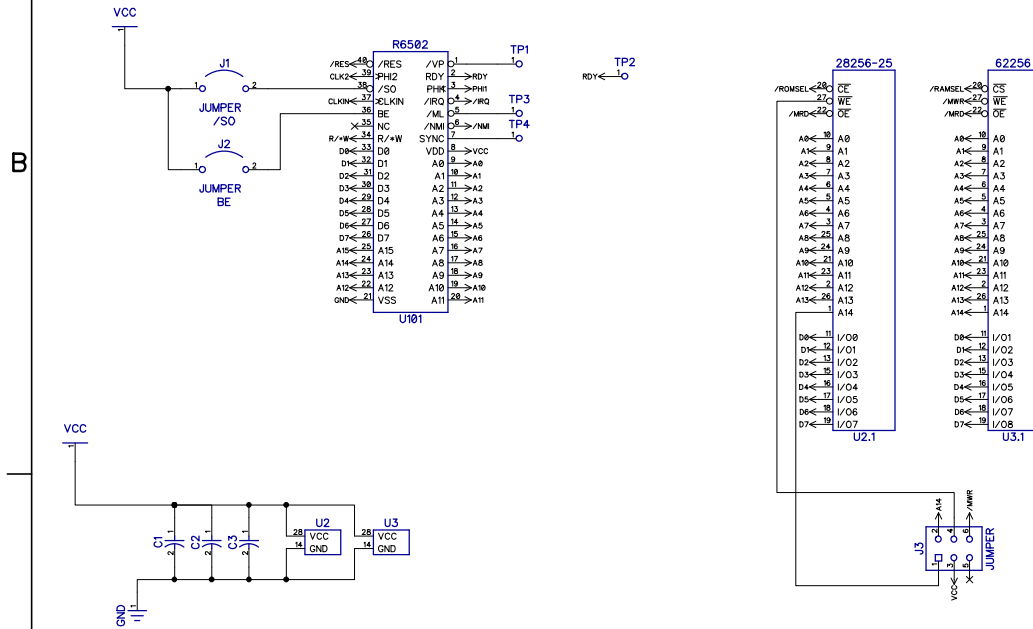


2

1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



A

A

2

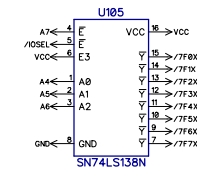
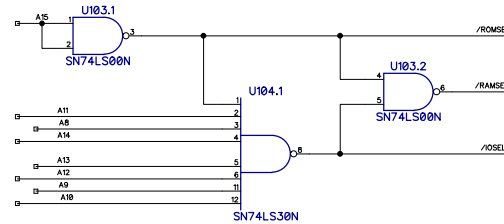
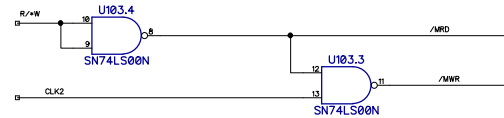
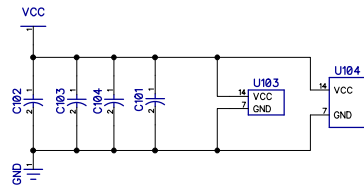
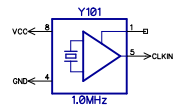
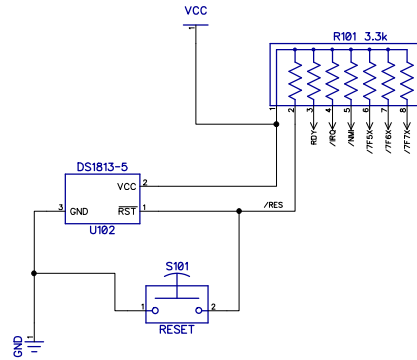
1

6502SBC Original: Daryl Rictor (2005) Redesign: Richard Cini (2014)			
SIZE A	FSCM NO.	DWG NO.	REV 27R1
SCALE	3/1/2014	CPU and Memory	

2

1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



6502SBC
Original: Daryl Rictor (2005)
Redesign: Richard Cini (2014)

SIZE	FSCM NO.	DWG NO.	REV
A			27R1
SCALE	3/1/2014	Clock and Decode	

2

1

2

1

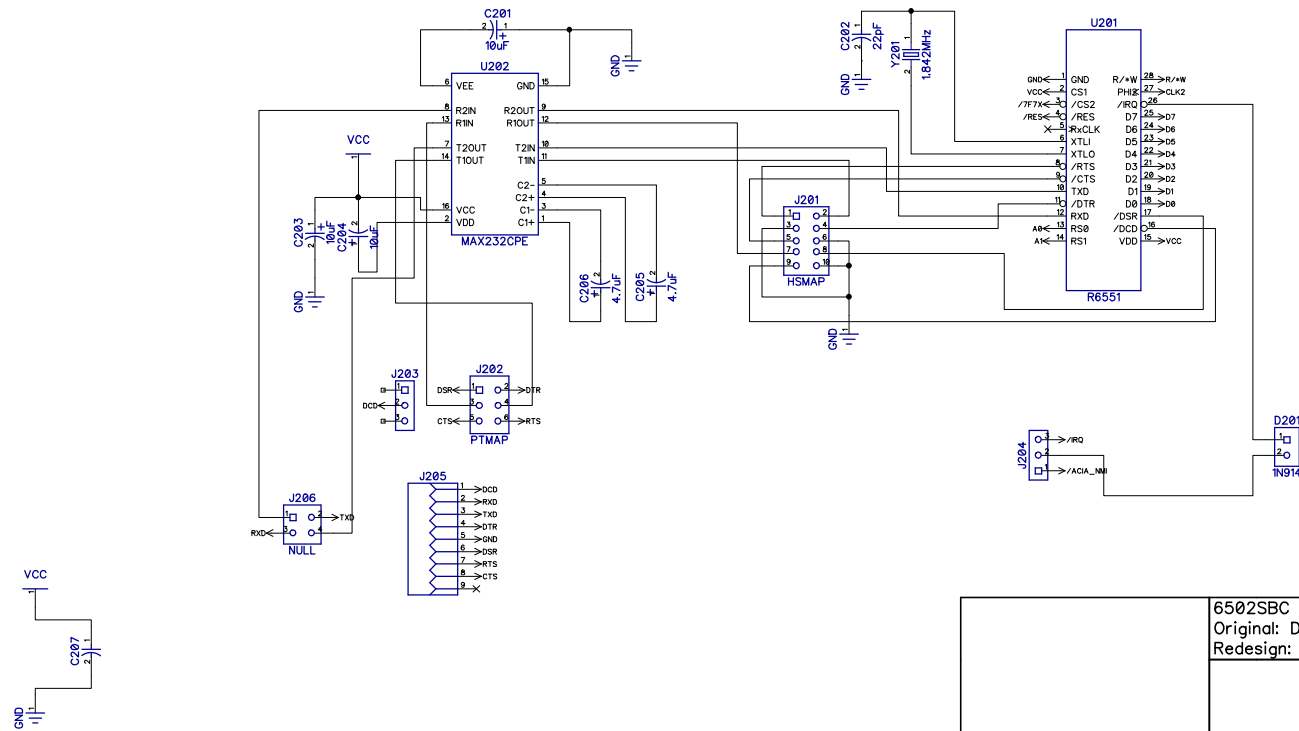
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

B

B

A

A

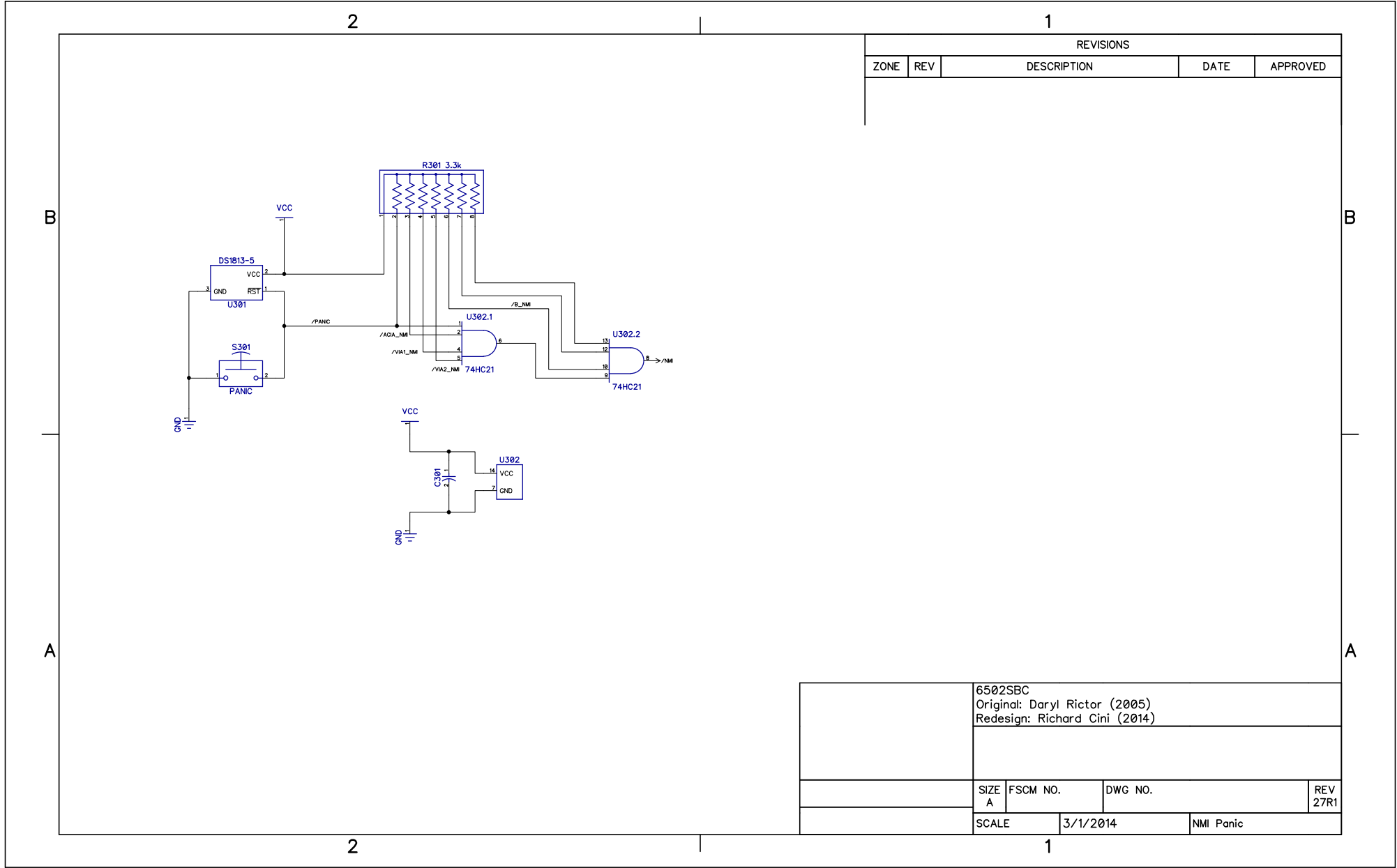


6502SBC
Original: Daryl Rictor (2005)
Redesign: Richard Cini (2014)

SIZE	FSCM NO.	DWG NO.	REV
A			27R1
SCALE		3/1/2014	ACIA1

2

1



2

1

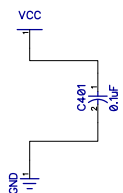
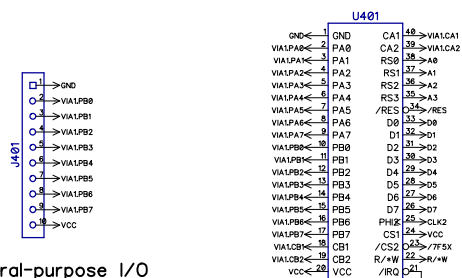
VIA for system use

All of PortA and CB1/CB2 used for IEC and Joystick

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

B

B



A

A

2

1

6502SBC
Original: Daryl Rictor (2005)
Redesign: Richard Cini (2014)

SIZE	FSCM NO.	DWG NO.	REV
A			27R1
SCALE	3/1/2014	VIA1	

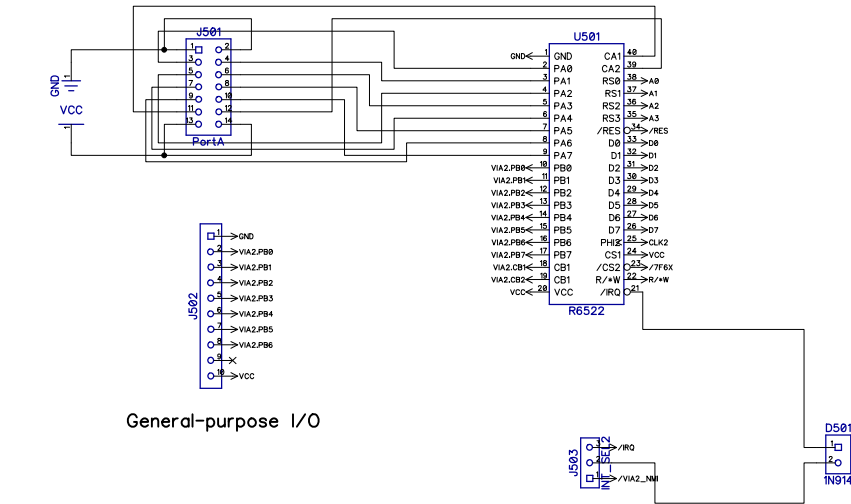
2

1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

B

B



General-purpose I/O

A

A

2

1

6502SBC Original: Daryl Rictor (2005) Redesign: Richard Cini (2014)			
SIZE A	FSCM NO.	DWG NO.	REV 27R1
SCALE	3/1/2014	VIA2	

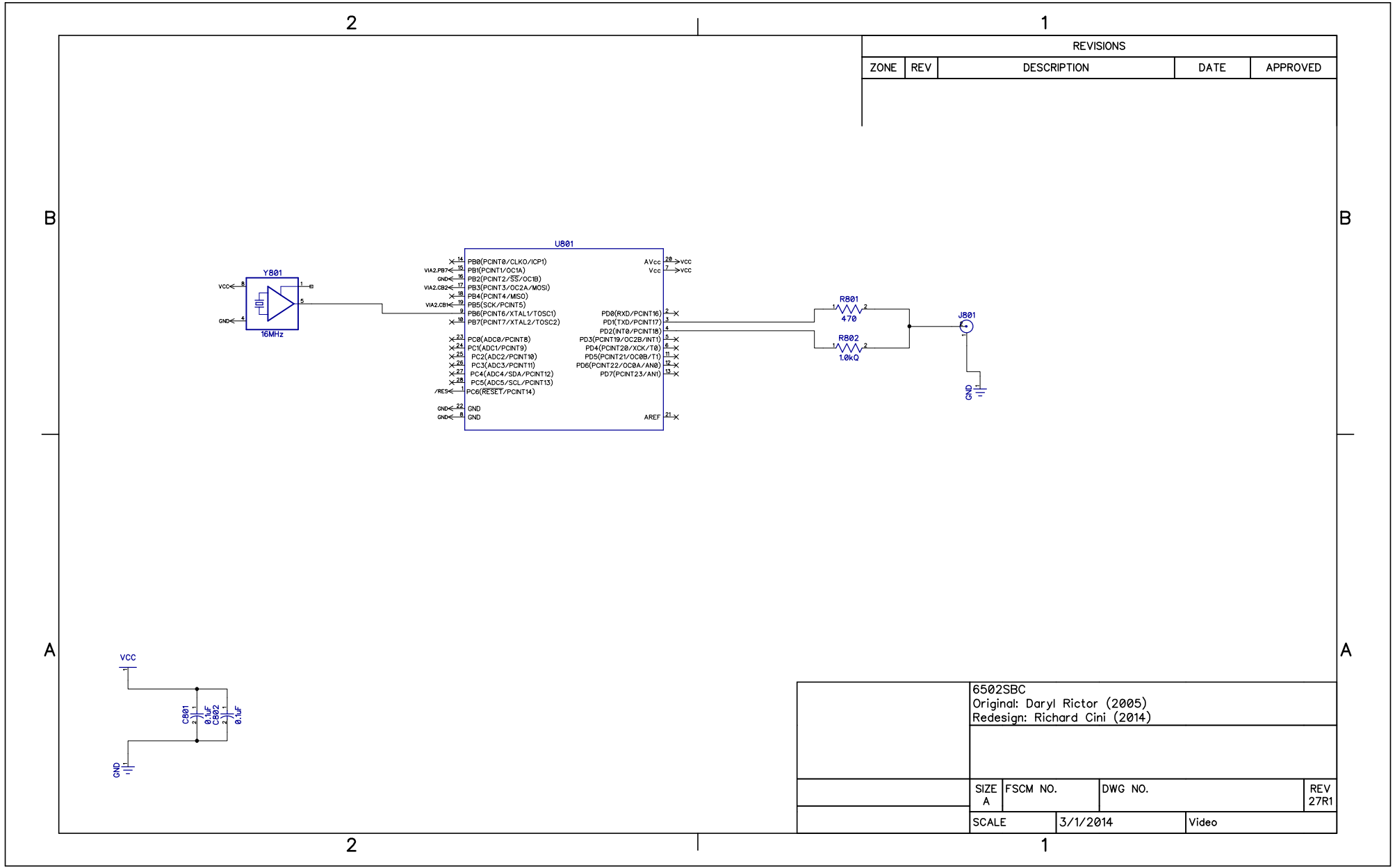
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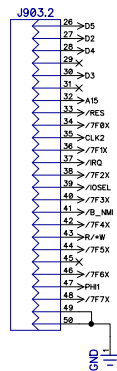
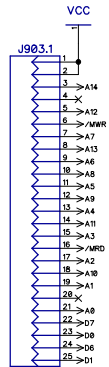
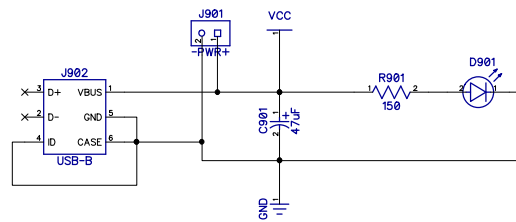
[illegible]

1=JOY_U 2=JOY_D
3=JOY_L 4=JOY_R
6=JOY_F
8=GND

2

1





REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
6/6/2014: Added PH1 to expansion connector.				

6502SBC
Original: Daryl Rictor (2005)
Redesign: Richard Cini (2014)

SIZE	FSCM NO.	DWG NO.	REV
A			27R1
SCALE		3/1/2014	Power and Expansion