PROOF OF CONCEPT V1

SINGLE-BOARD COMPUTER

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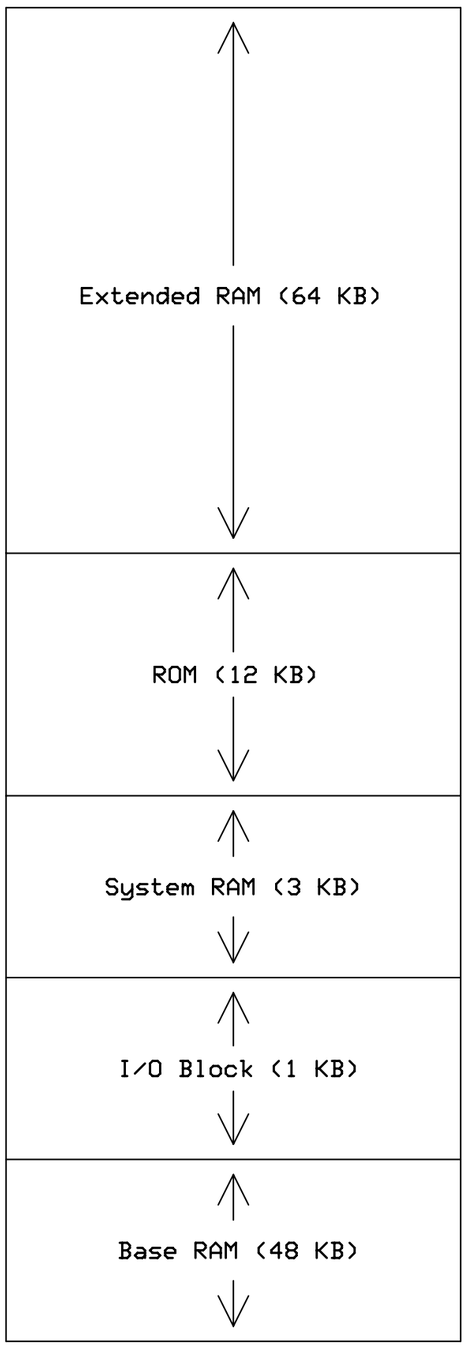
128 Kilobyte Static RAM System

Powered by the W65C816S Microprocessor

Designed by BigDumbDinosaur


$01FFFF
Extended RAM (64 KB)
$010000
ROM (12 KB)
$00D000
System RAM (3 KB)
$00C400
I/O Block (1 KB)
$00C000
Base RAM (48 KB)
$000000

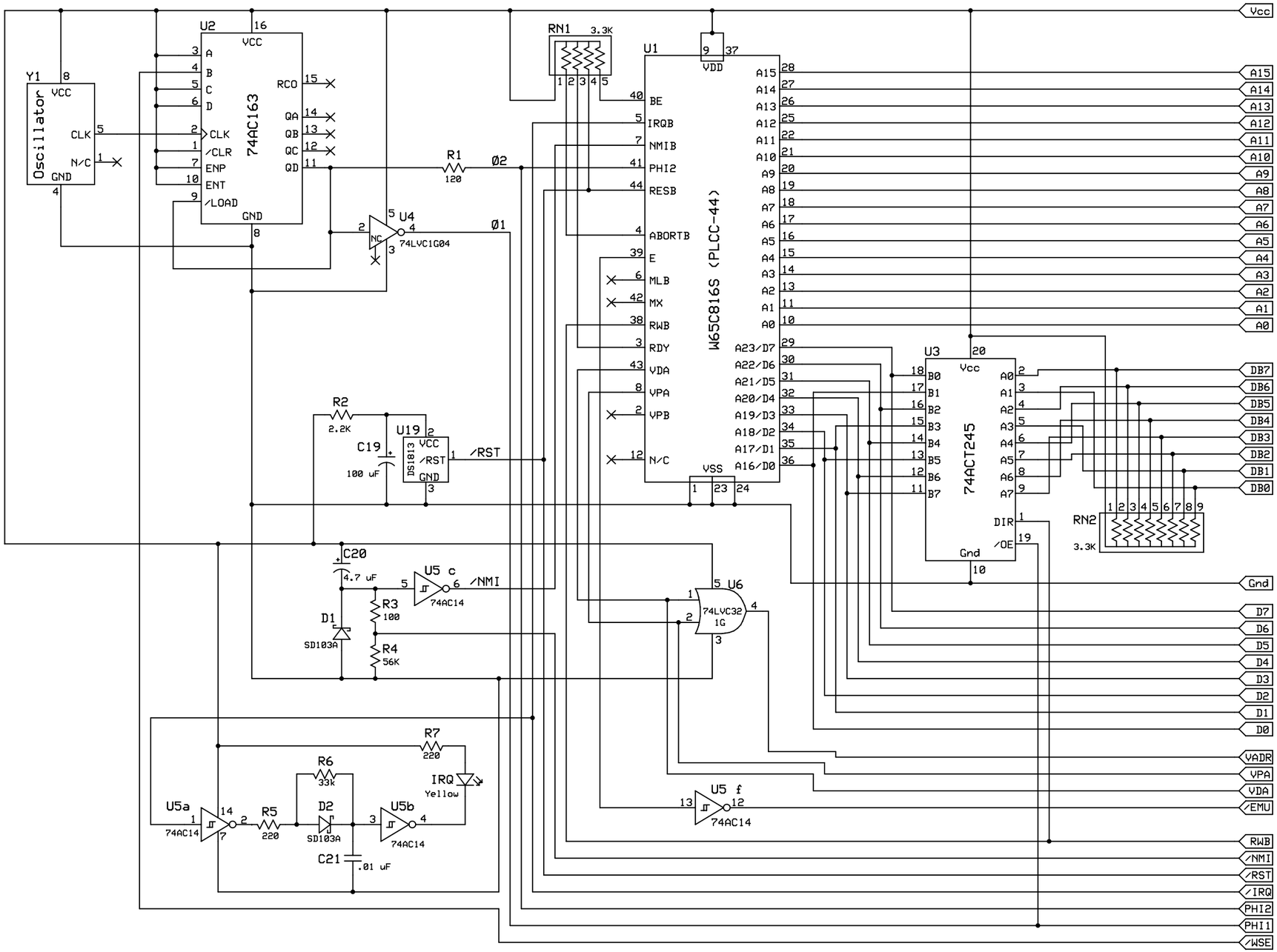
POC V1.4 MEMORY MAP

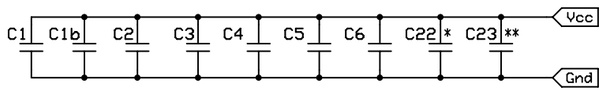
ADDRESS	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	SYMBOL	ASSIGNMENT	SIZE KB
$000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BASRAM	Base RAM Start	48.00
$00BFFF	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1		Base RAM End	
$00C000	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IOBLK (1)	I/O Start	1.00
$00C3FF	0	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1		I/O End	
$00C400	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	SYSRAM	System RAM Start	3.00
$00CFFF	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1		System RAM End	
$00D000	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	ROM	ROM Start	12.00
$00FFFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		ROM End	
$010000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EXRAM	Extended RAM Start	64.00
$01FFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		Extended RAM End	

1) 128 bytes assigned per I/O slot. $00C380-00C3FF unused.

I/O BLOCK DECODING

	8	4	2	1	0	0	0	0		
	0	0	0	0	8	4	2	1		
	0	0	0	0	0	0	0	0		
	0	0	0	0	0	0	0	0		
ADDRESS	A15	A14	A13	A12	A11	A10	A9	A8	ASSIGNMENT	SYM
$00C000	1	1	0	0	0	0	0	0	DUART #1 (chans A-B, timer A)	SIOA
$00C080	1	1	0	0	0	0	0	1	DUART #2 (chans C-D, timer B)	SIOB
$00C100	1	1	0	0	0	0	1	0	vQUART Channel IRQ Status	SIOQ
$00C180	1	1	0	0	0	0	1	1	Real-Time Clock & NVRAM	RTC
$00C200	1	1	0	0	0	1	0	0	Expansion Select A	XIOA
$00C280	1	1	0	0	0	1	0	1	Expansion Select B	XIOB
$00C300	1	1	0	0	0	1	1	0	Expansion Select C	XIOC





Decoupling Capacitors -- 0.1 uf @ 50v

*C22→Y1 **C23→RN2

MPU INTERFACE

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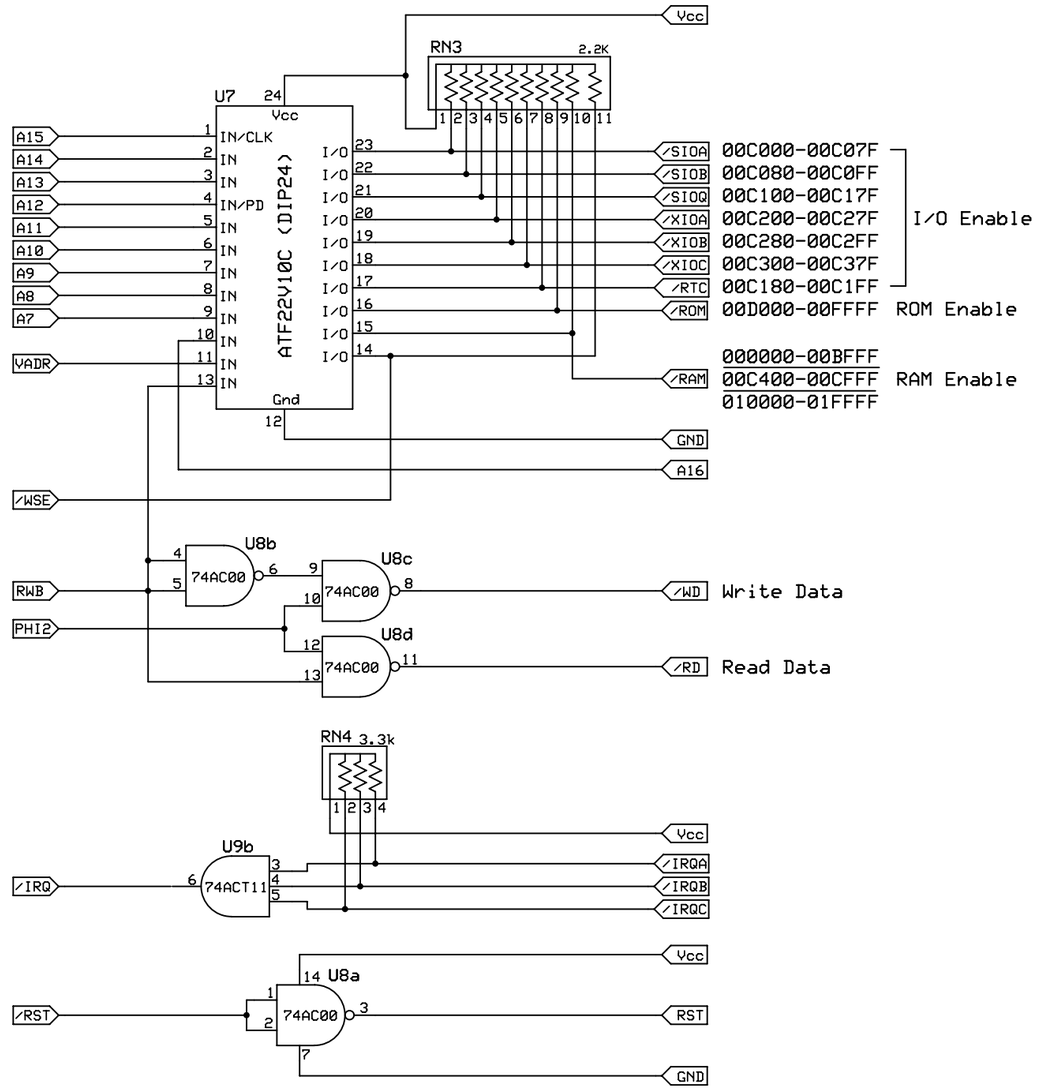

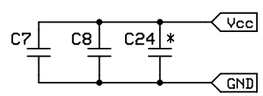

Decoupling Capacitors -- 0.1 uf @ 50v

*C24 → RN4

Use TE Connectivity 1-2199298-8 socket with U7.

GLUE LOGIC

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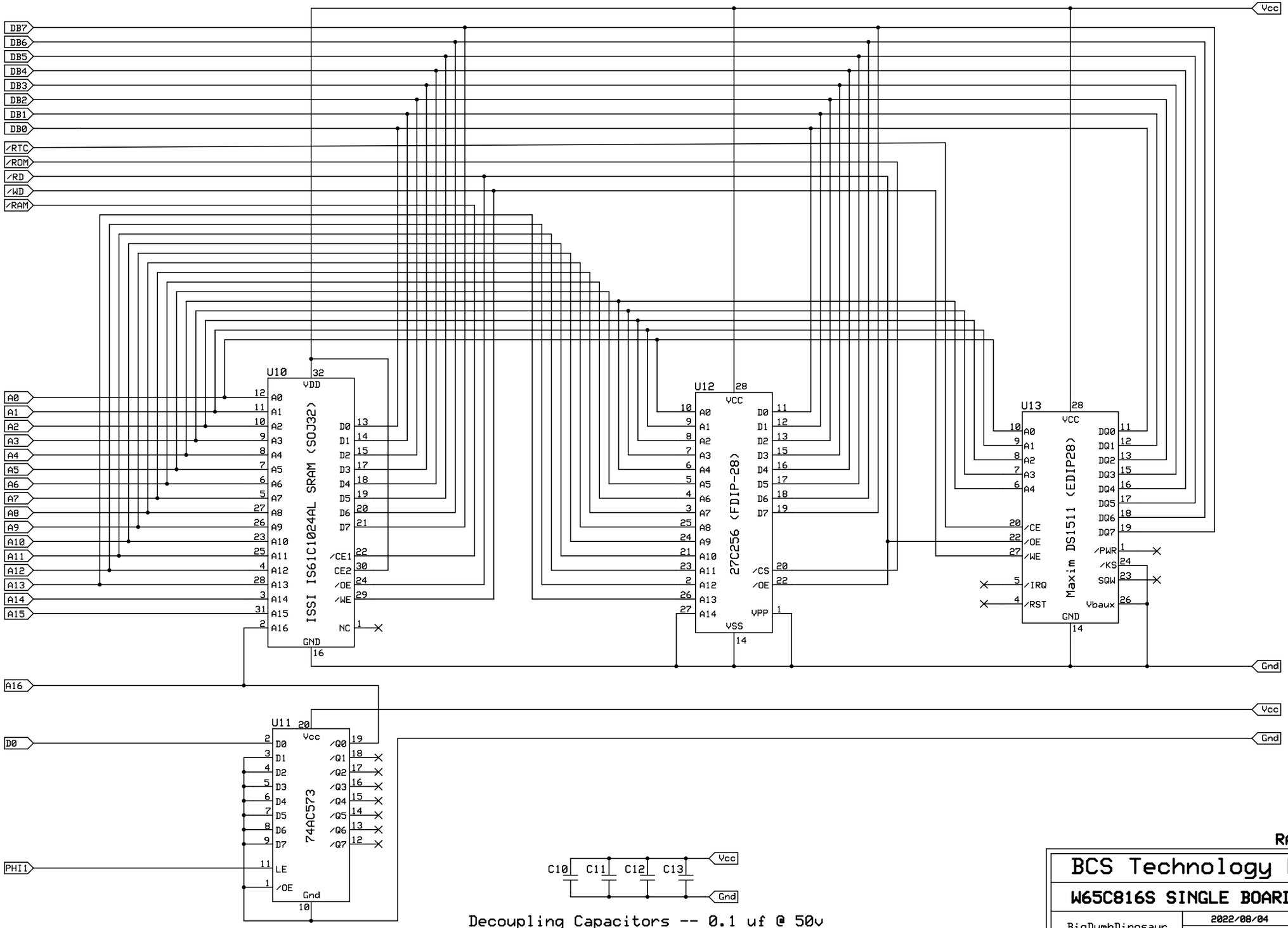
Vcc
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
/RTC
/ROM
/RD
/WD
/RAM
U10
32
VDD
ISSI IS61C1024AL SRAM (SOJ32)
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
D0
D1
D2
D3
D4
D5
D6
D7
/CE1
CE2
/OE
/WE
NC
GND
16
U12
28
VCC
27C256 (FDIP-28)
/CS
/OE
VPP
VSS
14
U13
28
VCC
Maxim DS1511 (EDIP28)
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
/CE
/OE
/WE
/IRQ
/RST
/PWR
/KS
SQW
Vbaux
GND
14
Gnd
Vcc
U11
20
74AC573
/Q0
/Q1
/Q2
/Q3
/Q4
/Q5
/Q6
/Q7
LE
/OE
Gnd
10
PHI1
C10
C11
C12
C13
Decoupling Capacitors -- 0.1 uf @ 50v
RAM, ROM & RTC
BCS Technology Limited
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BigDumbDinosaur
2022/08/04
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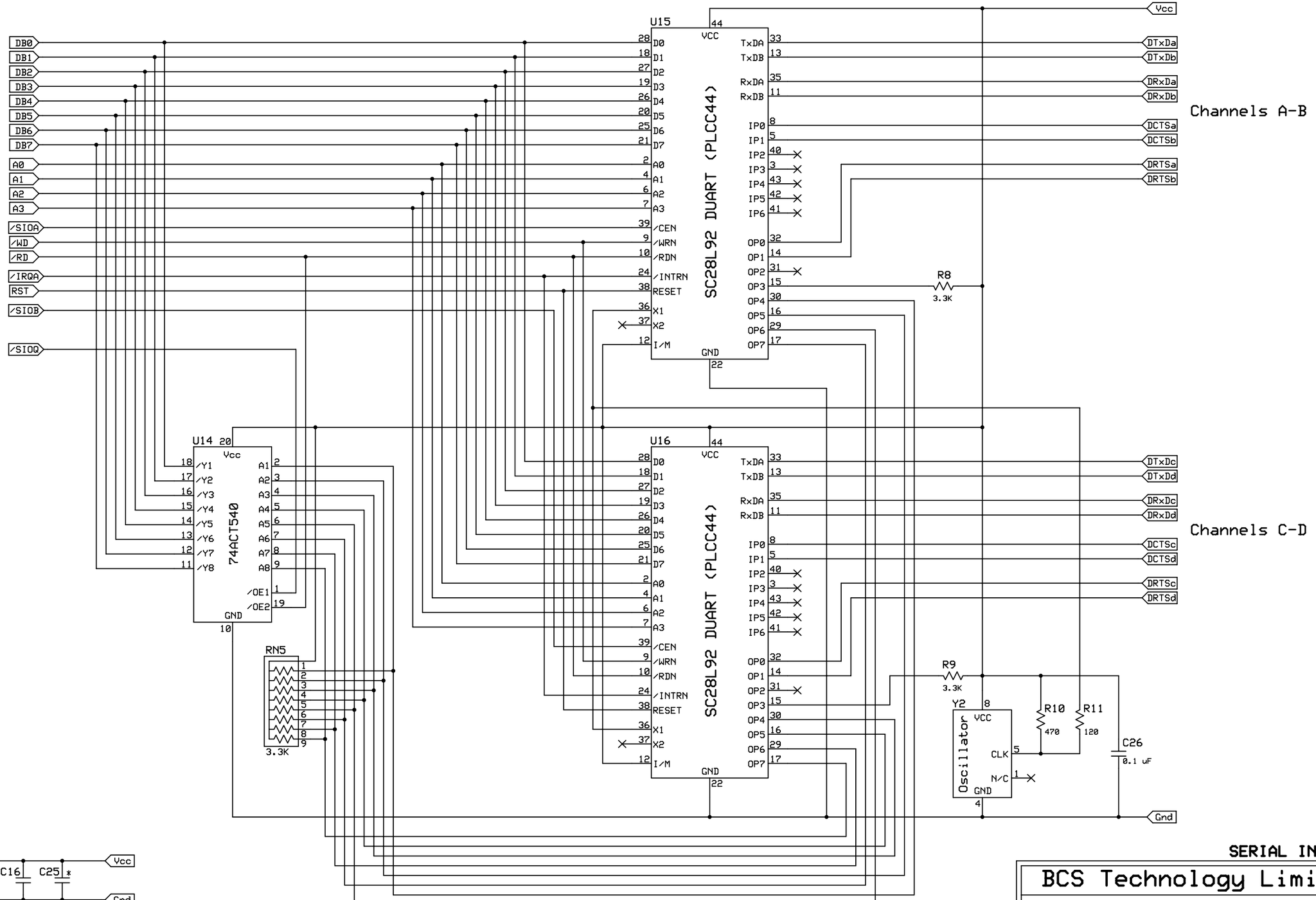
U15
SC28L92 DUART (PLCC44)
VCC
GND
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
/CEN
/WRN
/RDN
/INTRN
RESET
X1
X2
I/M
TxDA
TxDB
RxDA
RxDB
IP0
IP1
IP2
IP3
IP4
IP5
IP6
OP0
OP1
OP2
OP3
OP4
OP5
OP6
OP7
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
A0
A1
A2
A3
/SIOA
/WD
/RD
/IRQA
RST
/SIOB
/SIOQ
Vcc
DTxDa
DTxDb
DRxDa
DRxDb
DCTSa
DCTSb
DRTSa
DRTSb
R8
3.3K
Channels A-B
U14
74ACT540
/Y1
/Y2
/Y3
/Y4
/Y5
/Y6
/Y7
/Y8
A1
A2
A3
A4
A5
A6
A7
A8
/OE1
/OE2
RN5
U16
DTxDc
DTxDd
DRxDc
DRxDd
DCTSc
DCTSd
DRTSc
DRTSd
Channels C-D
R9
Y2
Oscillator
CLK
N/C
R10
470
R11
120
C26
0.1 uF
Gnd
C14
C15
C16
C25 *
Decoupling Capacitors -- 0.1 uf @ 50v
*C25→RN5
SERIAL INTERFACE
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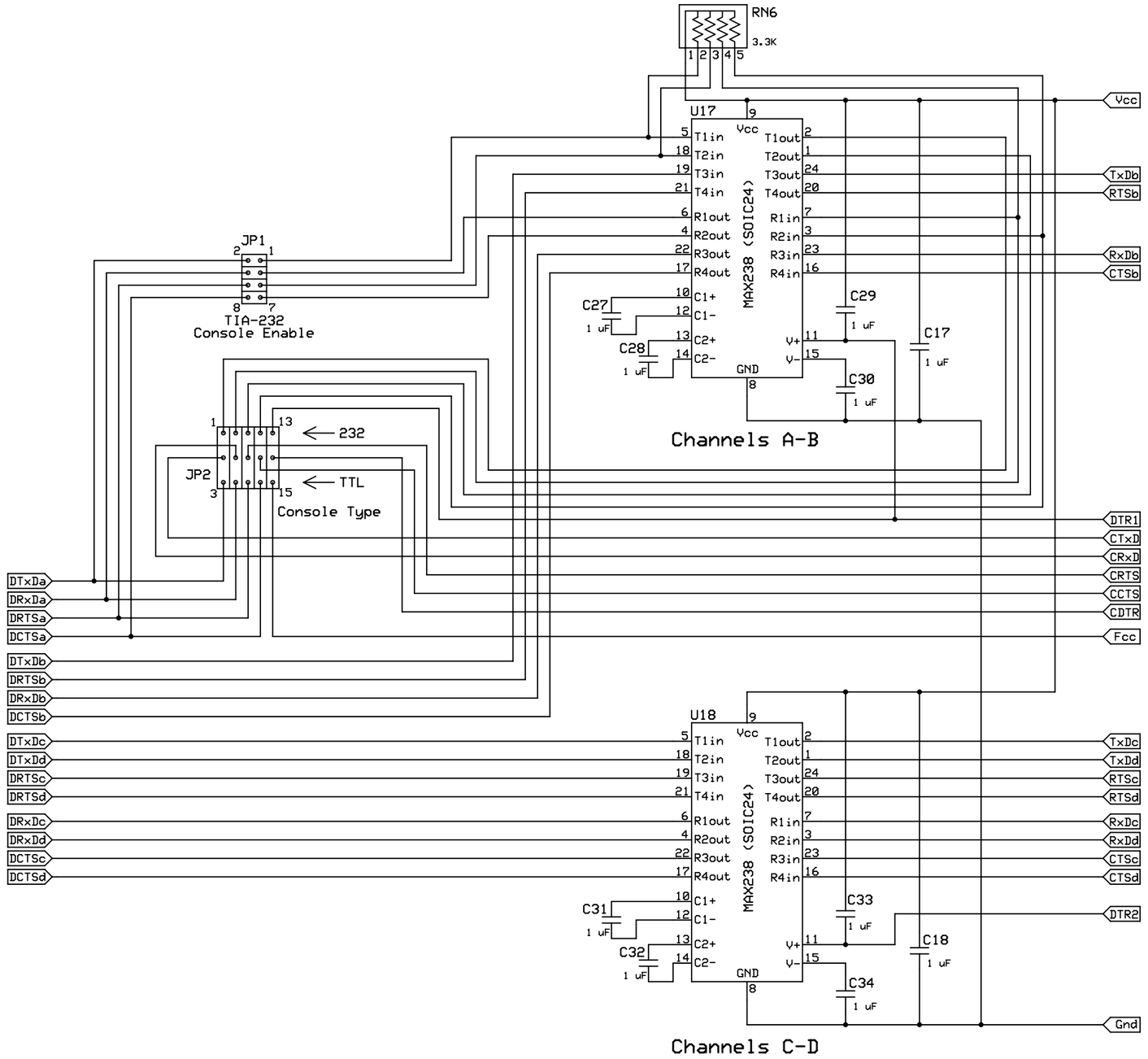

TIA-232 INPUT/OUTPUT

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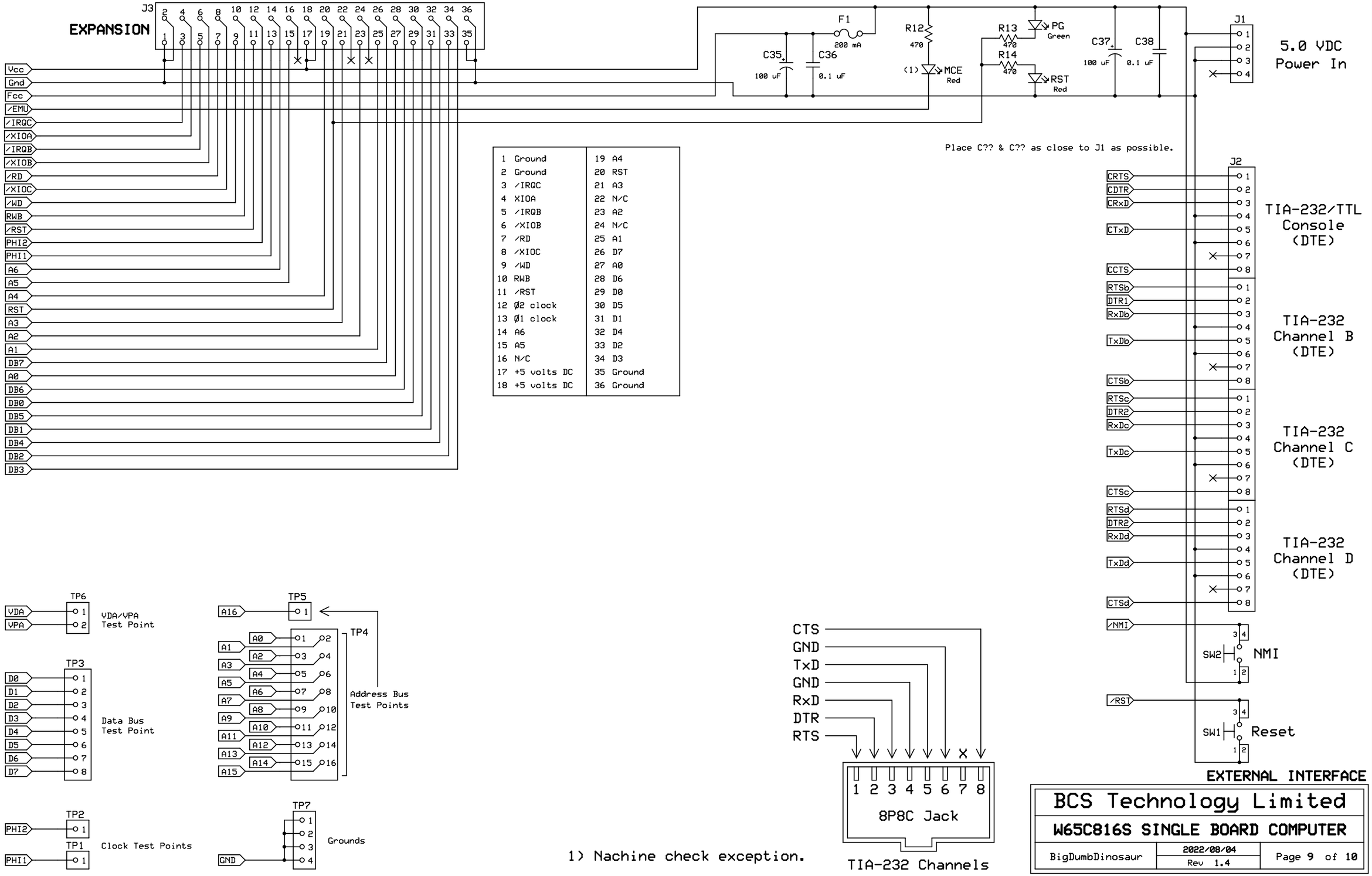

1	Ground	19	A4
2	Ground	20	RST
3	/IRQC	21	A3
4	XIOA	22	N/C
5	/IRQB	23	A2
6	/XIOB	24	N/C
7	/RD	25	A1
8	/XIOC	26	D7
9	/WD	27	A0
10	RWB	28	D6
11	/RST	29	D0
12	Ø2 clock	30	D5
13	Ø1 clock	31	D1
14	A6	32	D4
15	A5	33	D2
16	N/C	34	D3
17	+5 volts DC	35	Ground
18	+5 volts DC	36	Ground

1) Nachine check exception.

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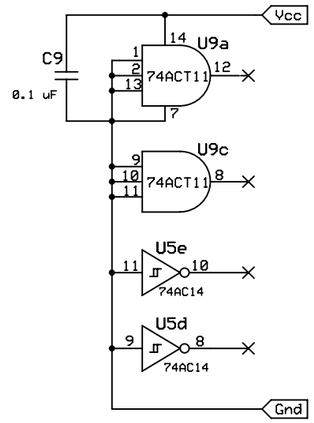

SPARE GATES

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