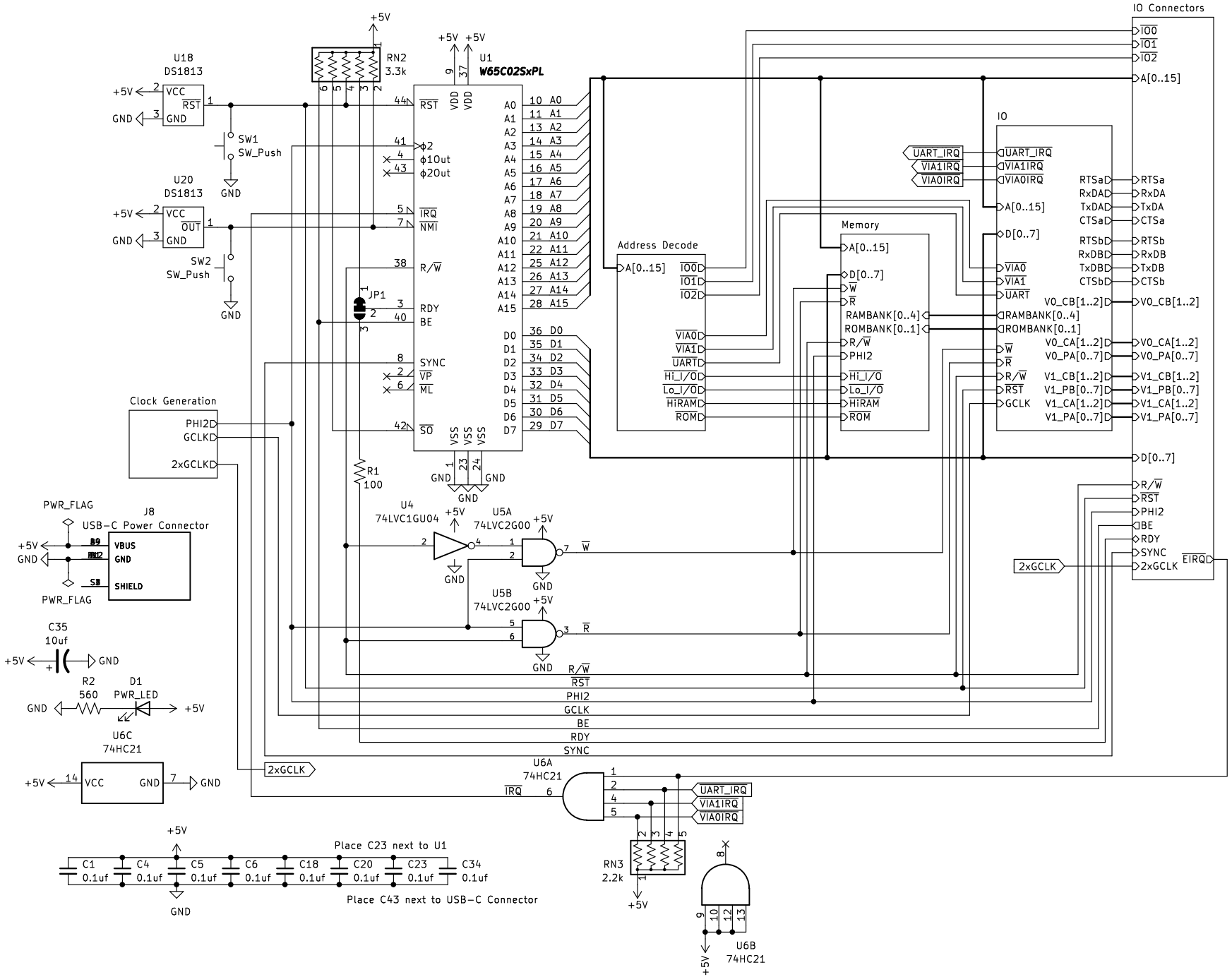
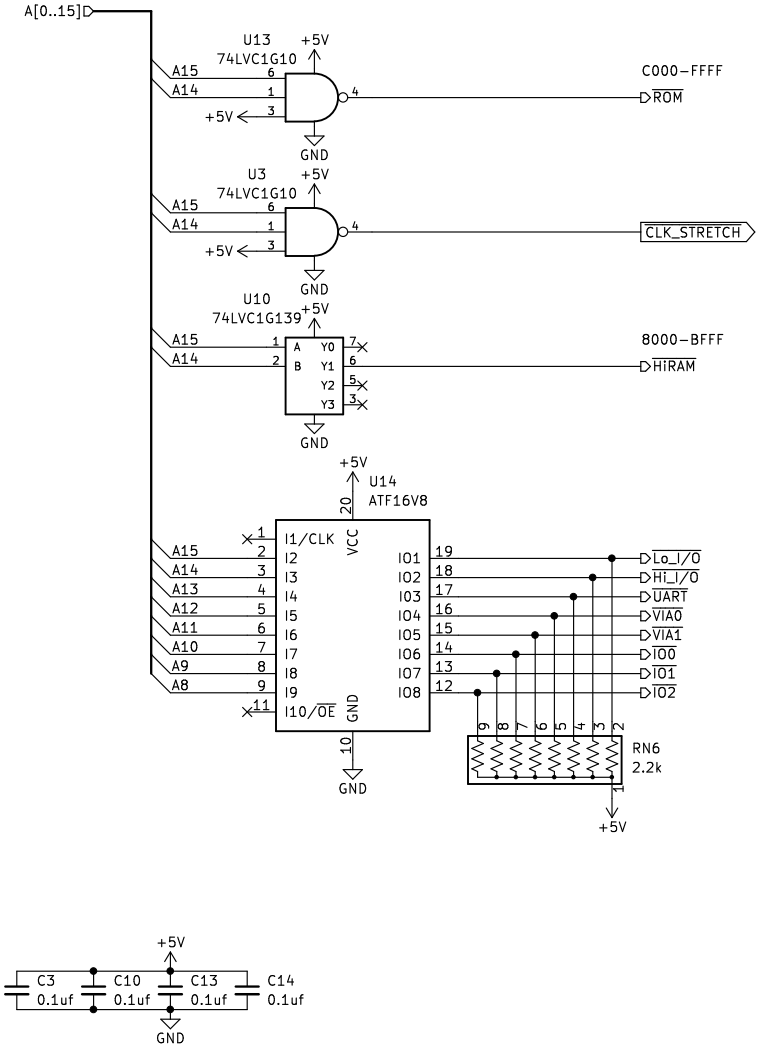
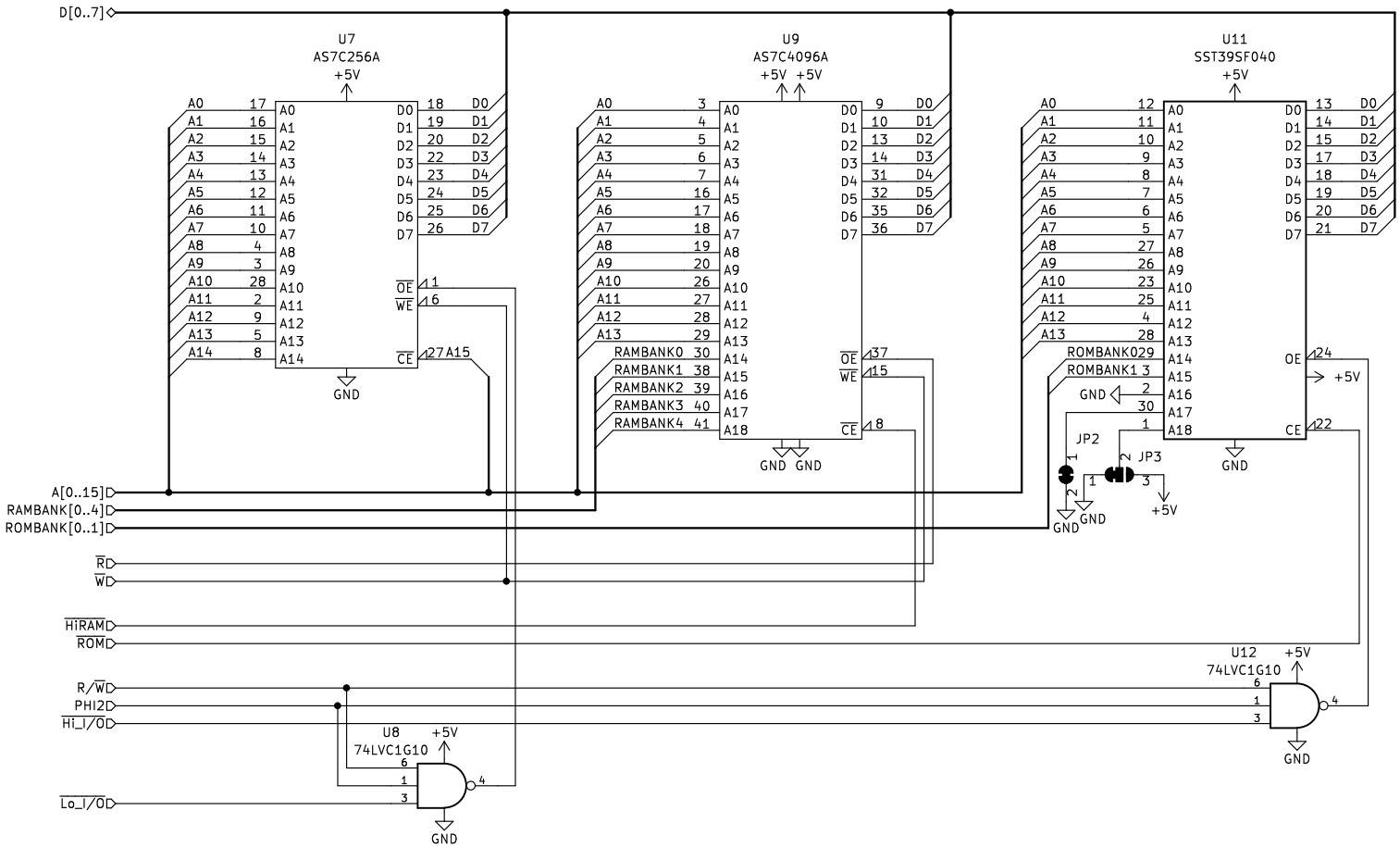
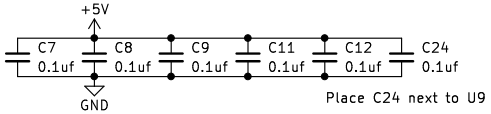
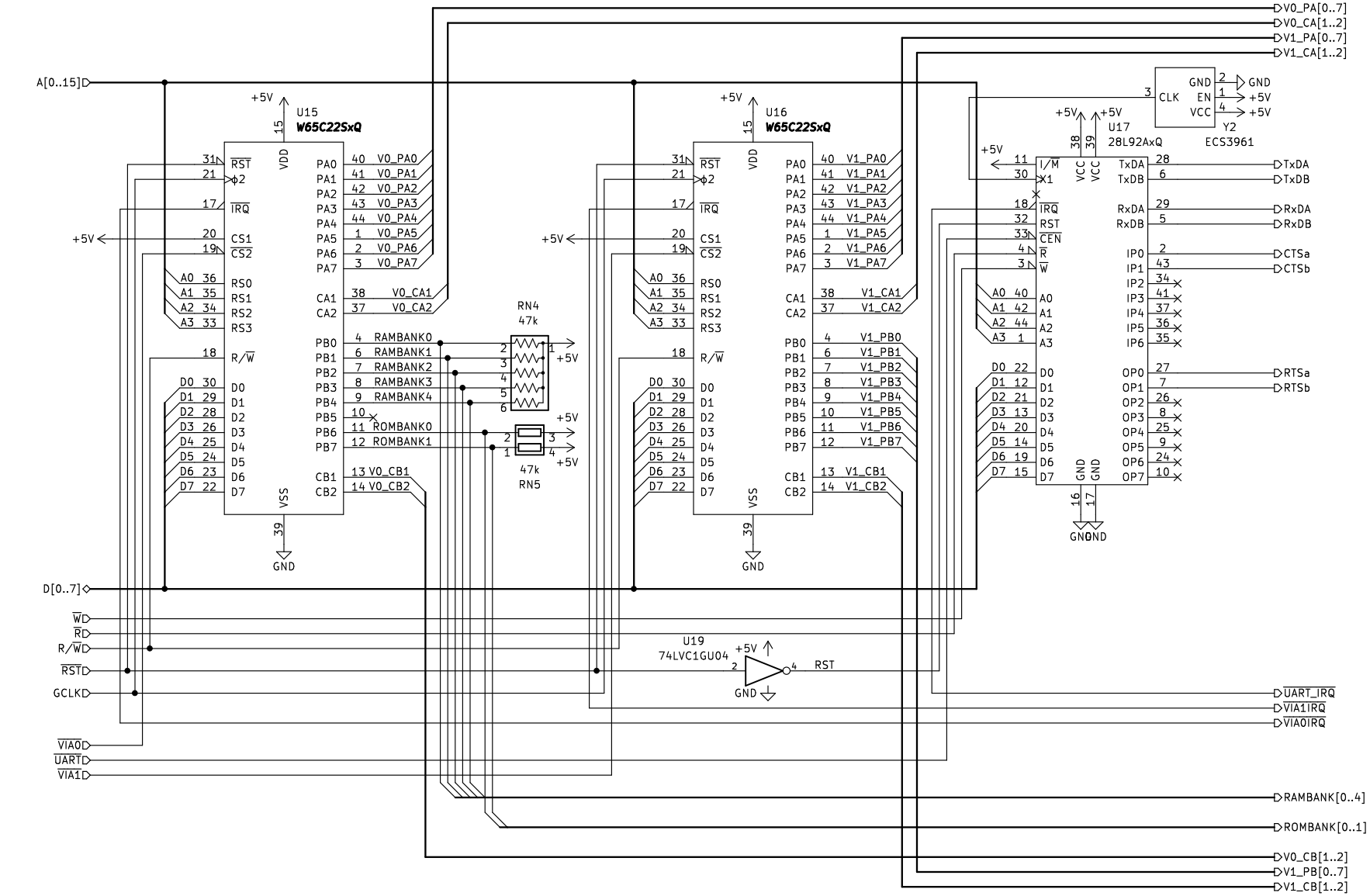

U18
DS1813
U20
DS1813
SW1
SW_Push
SW2
SW_Push
RN2
3.3k
U1
W65C02SxPL
JP1
R1
100
Clock Generation
PHI2
GCLK
2xGCLK
PWR_FLAG
J8
USB-C Power Connector
VBUS
GND
SHIELD
C35
10uf
R2
560
D1
PWR_LED
U6C
74HC21
U4
74LVC1GU04
U5A
74LVC2GU00
U5B
74LVC2GU00
U6A
74HC21
U6B
74HC21
RN3
2.2k
C1 0.1uf
C4 0.1uf
C5 0.1uf
C6 0.1uf
C18 0.1uf
C20 0.1uf
C23 0.1uf
C34 0.1uf
Place C23 next to U1
Place C43 next to USB-C Connector
Address Decode
Memory
IO
IO Connectors
UART_IRQ
VIA1IRQ
VIA0IRQ
A[0..15]
D[0..7]
RAMBANK[0..4]
ROMBANK[0..1]
RTSa
RxDA
TxDA
CTSa
RTSb
RxDB
TxDB
CTSb
V0_CB[1..2]
V0_CA[1..2]
V0_PA[0..7]
V1_CB[1..2]
V1_PB[0..7]
V1_CA[1..2]
V1_PA[0..7]
EIRQ

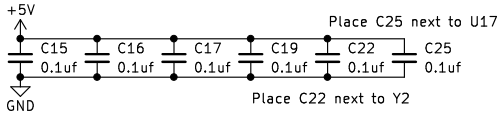

A[0..15]
U13
74LVC1G10
+5V
A15
A14
C000-FFFF
ROM
GND
U3
74LVC1G10
CLK_STRETCH
U10
74LVC1G139
A
B
Y0
Y1
Y2
Y3
8000-BFFF
HIRAM
U14
ATF16V8
I1/CLK
I2
I3
I4
I5
I6
I7
I8
I9
I10/OE
VCC
GND
A13
A12
A11
A10
A9
A8
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
Lo_I/O
Hi_I/O
UART
VIA0
VIA1
IO0
IO1
IO2
RN6
2.2k

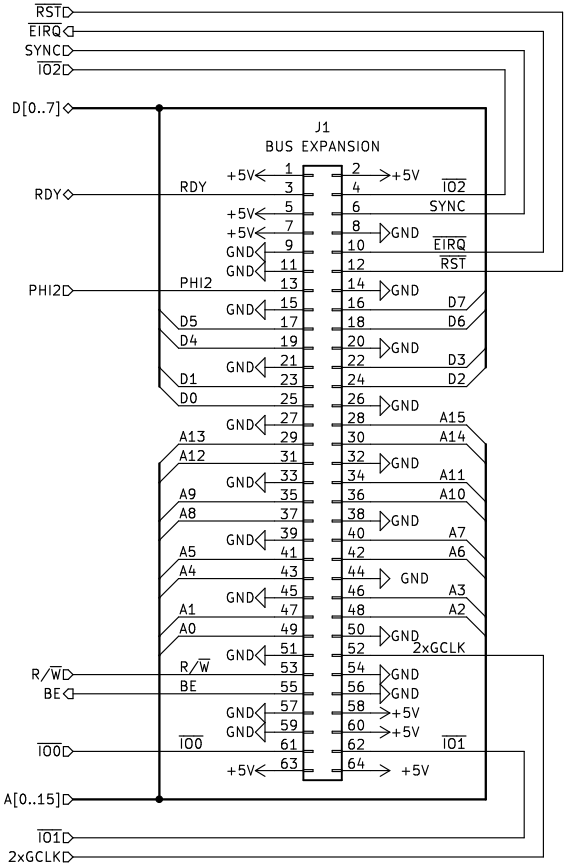

+5V
C3
0.1uf
C10
0.1uf
C13
0.1uf
C14
0.1uf
GND

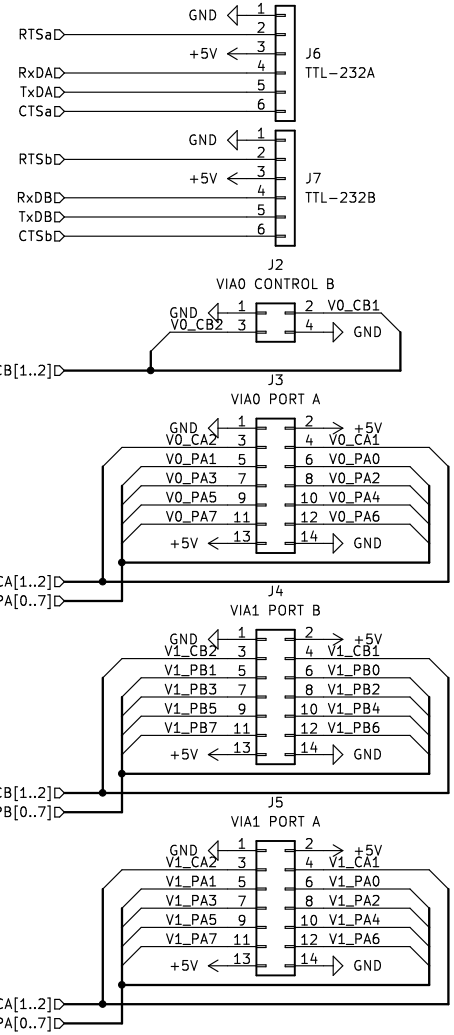

D[0..7]
U7
AS7C256A
+5V
U9
AS7C4096A
+5V +5V
U11
SST39SF040
+5V
A[0..15]
RAMBANK[0..4]
ROMBANK[0..1]
R
W
HiRAM
ROM
R/W
PHI2
Hi_I/O
Lo_I/O
U8
74LVC1G10
U12
74LVC1G10
JP2
JP3
GND
+5V

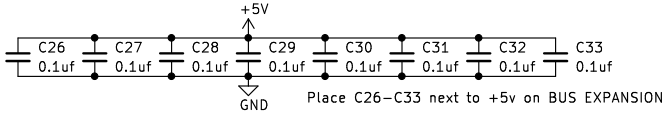

+5V
C7 0.1uf
C8 0.1uf
C9 0.1uf
C11 0.1uf
C12 0.1uf
C24 0.1uf
GND
Place C24 next to U9

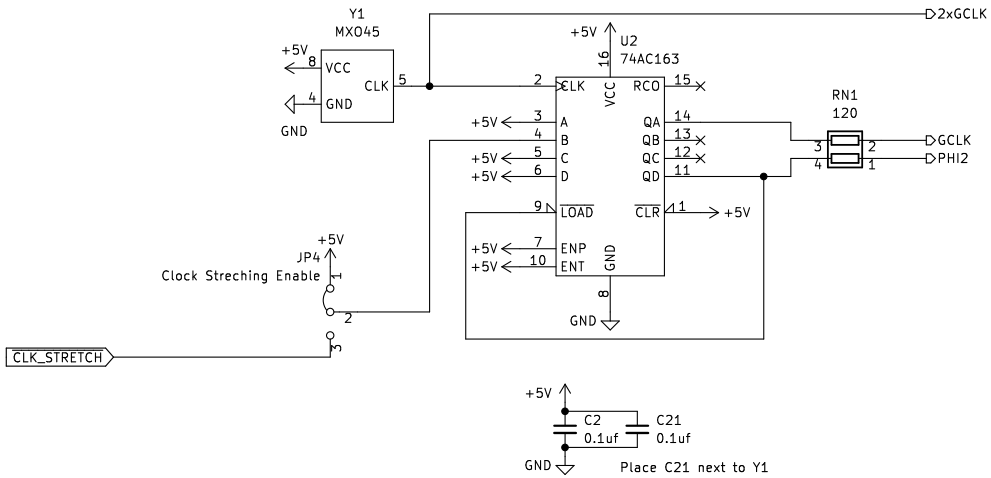

A[0..15]
D[0..7]
W
R
R/W
RST
GCLK
VIA0
UART
VIA1
U15
W65C22SxQ
U16
W65C22SxQ
U17
28L92AxQ
Y2
ECS3961
U19
74LVC1GU04
RN4
47k
RN5
47k
+5V
GND
V0_PA[0..7]
V0_CA[1..2]
V1_PA[0..7]
V1_CA[1..2]
TxDA
TxDB
RxDA
RxDB
CTSa
CTSb
RTSa
RTSb
UART_IRQ
VIA1IRQ
VIA0IRQ
RAMBANK[0..4]
ROMBANK[0..1]
V0_CB[1..2]
V1_PB[0..7]
V1_CB[1..2]


+5V
C15 0.1uf
C16 0.1uf
C17 0.1uf
C19 0.1uf
C22 0.1uf
C25 0.1uf
GND
Place C25 next to U17
Place C22 next to Y2


RST
EIRQ
SYNC
IO2
D[0..7]
RDY
PHI2
R/W
BE
IO0
A[0..15]
IO1
2xGCLK
J1
BUS EXPANSION


RTSa
RxDA
TxDA
CTSa
J6
TTL-232A
RTSb
RxDB
TxDB
CTSb
J7
TTL-232B
J2
VIA0 CONTROL B
V0_CB[1..2]
J3
VIA0 PORT A
V0_CA[1..2]
V0_PA[0..7]
J4
VIA1 PORT B
V1_CB[1..2]
V1_PB[0..7]
J5
VIA1 PORT A
V1_CA[1..2]
V1_PA[0..7]


+5V
C26 0.1uf
C27 0.1uf
C28 0.1uf
C29 0.1uf
C30 0.1uf
C31 0.1uf
C32 0.1uf
C33 0.1uf
GND
Place C26-C33 next to +5v on BUS EXPANSION


Y1
MX045
+5V
VCC
CLK
GND
2xGCLK
U2
74AC163
CLK
RCO
A
B
C
D
QA
QB
QC
QD
LOAD
CLR
ENP
ENT
VCC
GND
RN1
120
GCLK
PHI2
JP4
Clock Streching Enable
CLK_STRETCH
C2
0.1uf
C21
0.1uf
Place C21 next to Y1