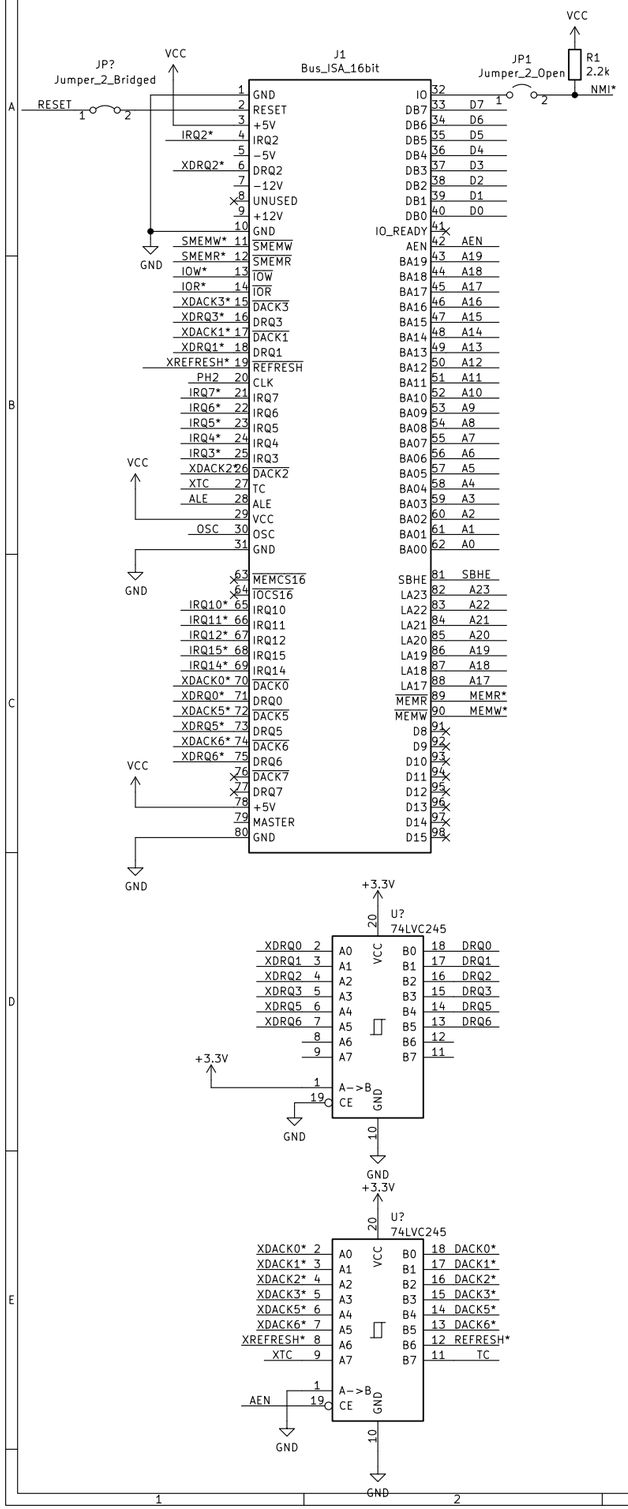

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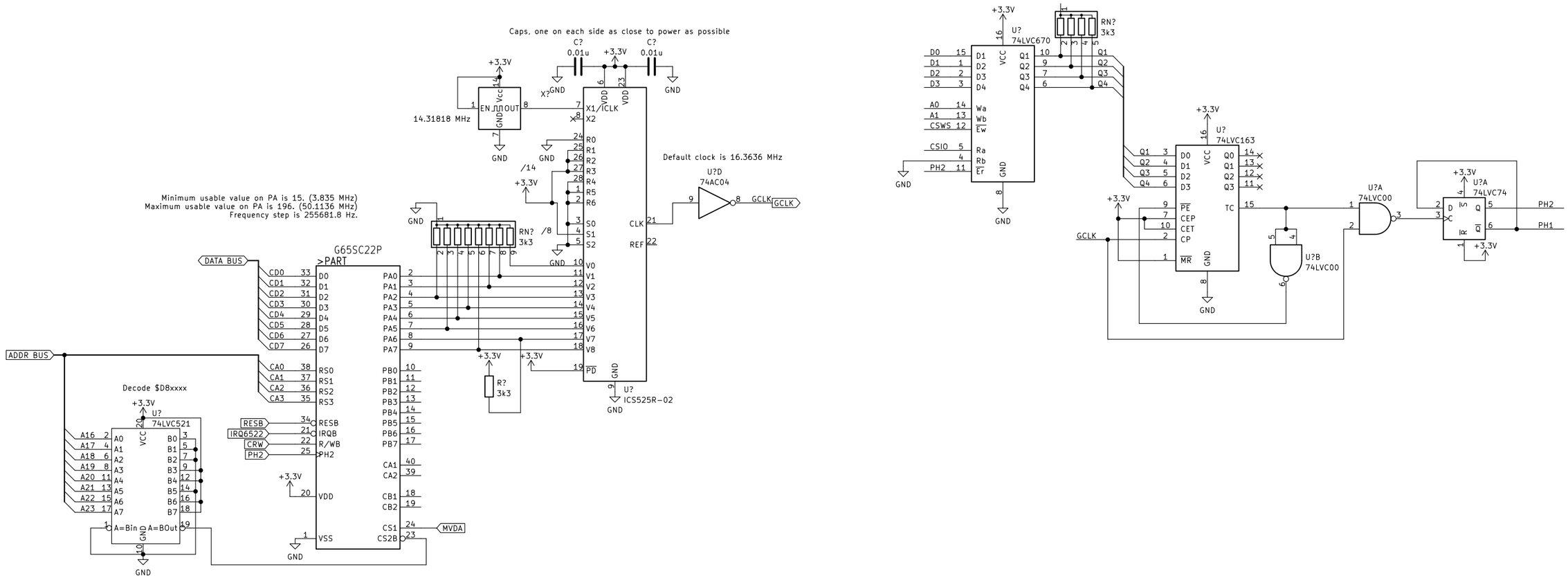
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.6)		Id: 1/4



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File: Clkgen.kicad_sch	
Title:	
Size: B	Date:
KiCad E.D.A. kicad (6.0.6)	Id: 2/4

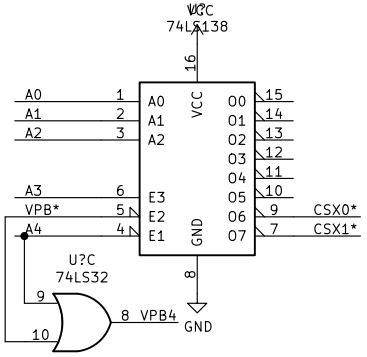
Interrupt request logic

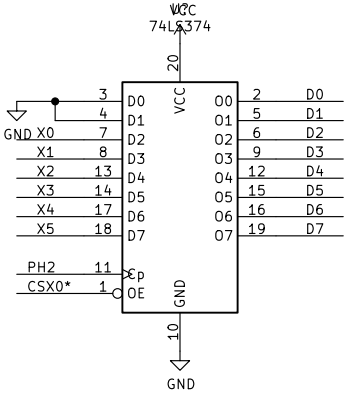
Located in the FPGA

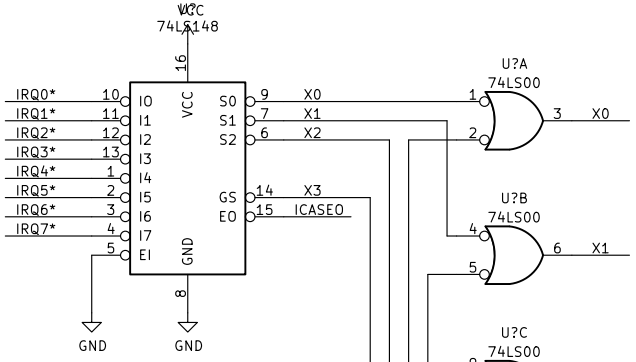
X4,X5 driven by addressable latch external to this circuit

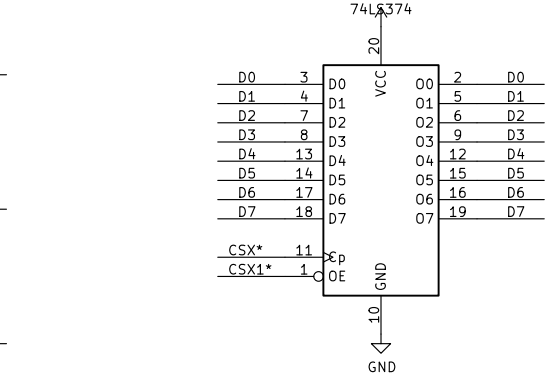
The vector pull operation in native mode accesses a pair of registers. The low order address bits are determined by the interrupt request level, spaced 4 bytes apart. The high order address bits come from a programmable latch. This allows any 64 byte region in the lower 64k bank to be selected as a vector target.

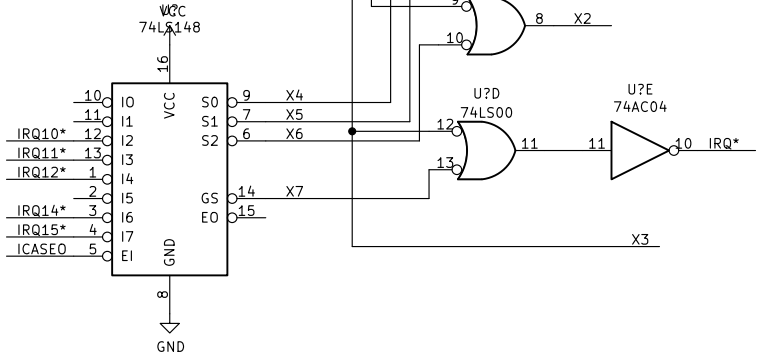
The VPB4 signal feeds into the ROM chip select logic to disable the ROM during a native mode vector fetch.







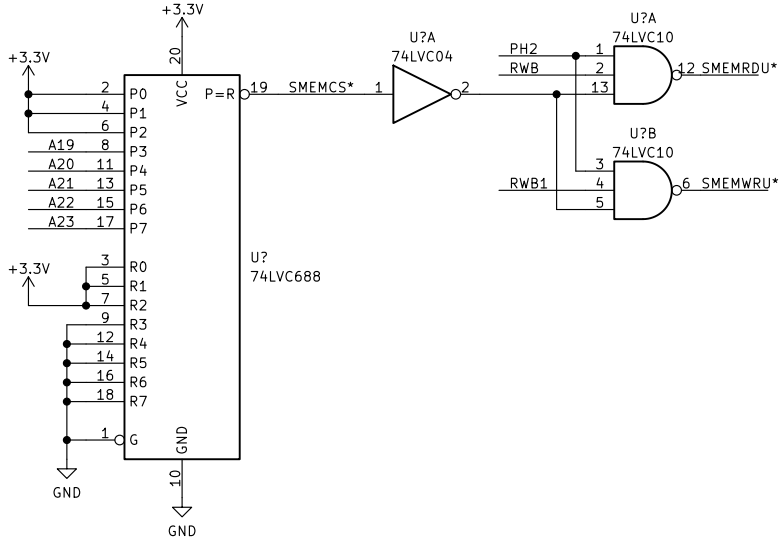


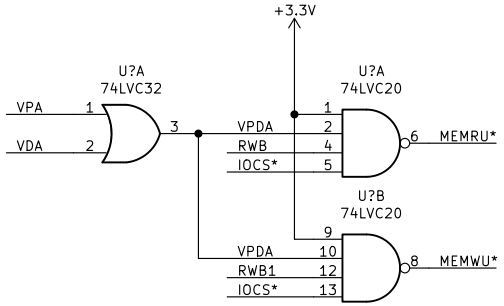


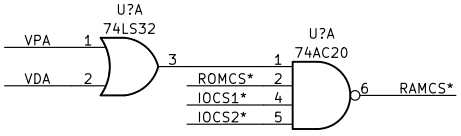
Sheet: /IRQ/ File: IRQ.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (6.0.6)		Id: 3/4

This logic internal to the FPGA

MEMWR is not qualified by the ROM chip select to allow writing to ram underneath the ROM.

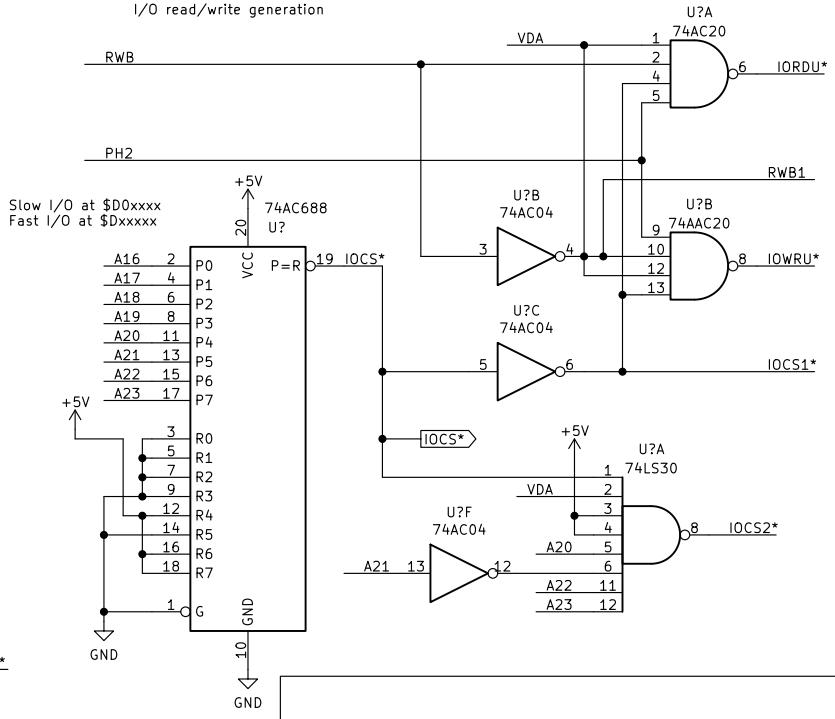






I/O read/write generation

Slow I/O at $D0xxxx
Fast I/O at $Dxxxxx



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Title:

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KiCad E.D.A. kicad (6.0.6)		Id: 4/4