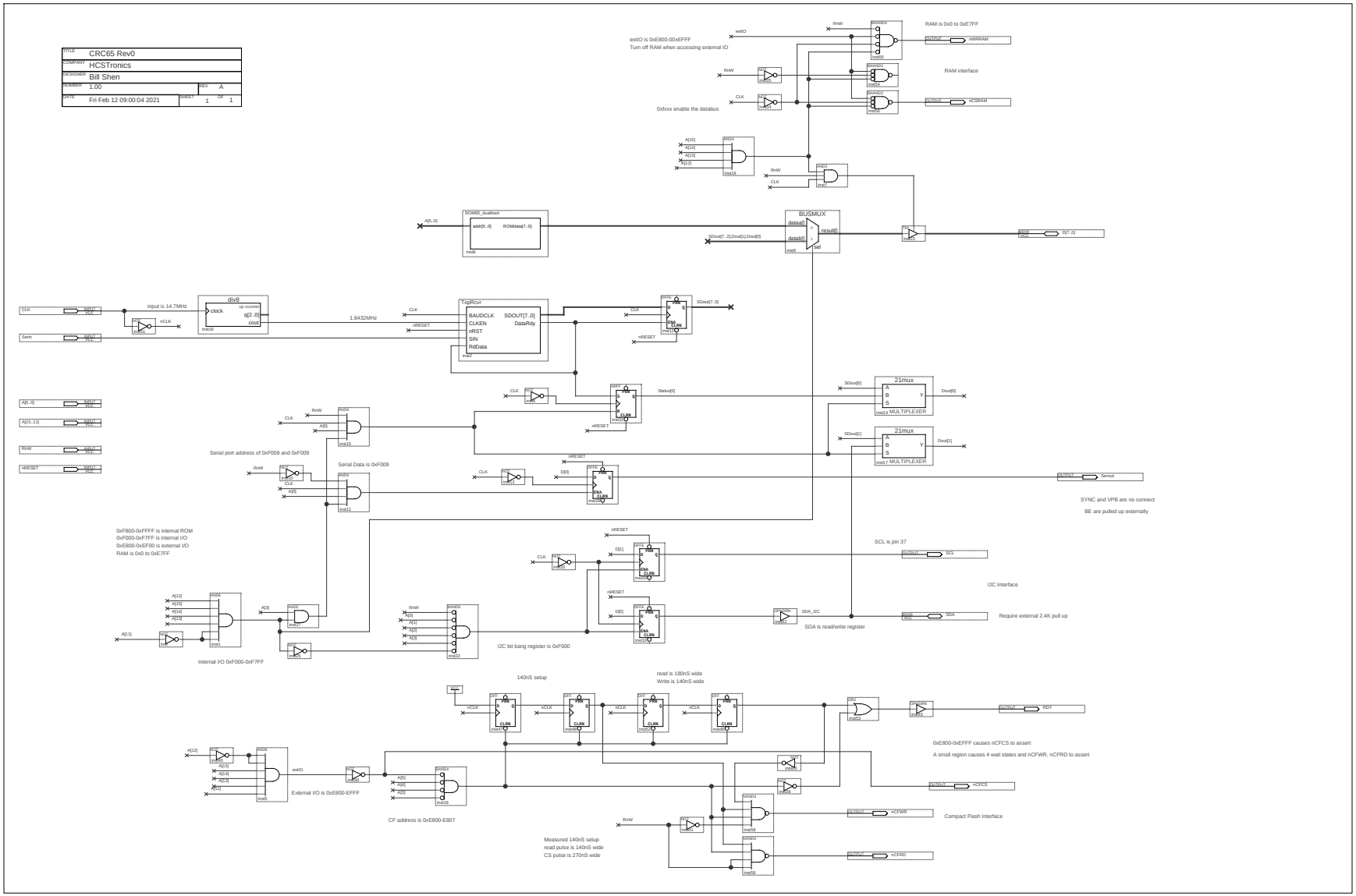
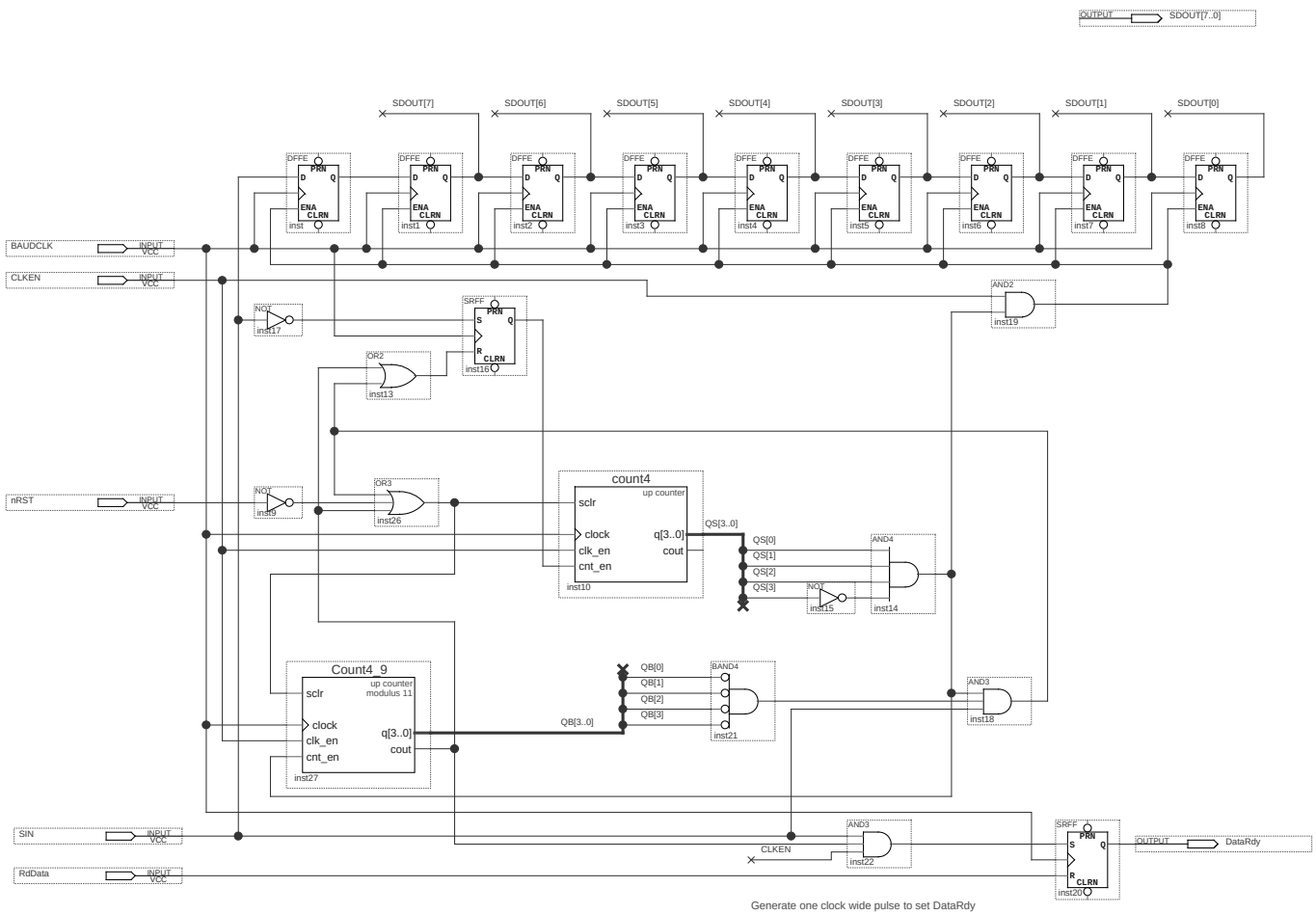

TITLE CRC65 Rev0
COMPANY HCSTronics
DESIGNER Bill Shen
NUMBER 1.00
REV A
DATE Fri Feb 12 09:00:04 2021
SHEET 1 OF 1
extIO is 0xE800-00xEFFF
Turn off RAM when accessing external IO
RAM is 0x0 to 0xE7FF
hWRRAM
RAM interface
hCSRAM
0xfxxx enable the databus
ROMB5_dualboot
ROMdata[7..0]
BUSMUX
D[7..0]
input is 14.7MHz
divB
1.8432MHz
TopRcvr
BAUDCLK
CLKEN
nRST
SIN
RxData
SDOUT[7..0]
DataRdy
SDout[7..0]
Serin
21mux
MULTIPLEXER
Serial port address of 0xF008 and 0xF009
Serial Data is 0xF009
Serout
SYNC and VPB are no connect
BE are pulled up externally
0xF800-0xFFFF is internal ROM
0xF000-0xF7FF is internal I/O
0xE800-0xEF00 is external I/O
RAM is 0x0 to 0xE7FF
SCL is pin 37
SCL
I2C Interface
SDA_I2C
SDA
Require external 2.4K pull up
SDA is read/write register
Internal I/O 0xF000-0xF7FF
I2C bit bang register is 0xF000
140nS setup
read is 180nS wide
Write is 140nS wide
RDY
0xE800-0xEFFF causes nCFCS to assert
A small region causes 4 wait states and nCFWR, nCFRD to assert
nCFCS
External I/O is 0xE800-EFFF
CF address is 0xEB00-EB07
Compact Flash Interface
nCFWR
nCFRD
Measured 140nS setup
read pulse is 140nS wide
CS pulse is 270nS wide



Generate one clock wide pulse to set DataRdy
Because DataRdy may generate an interrupt. If interrupt service occurred too quickly, the flipflop may still be setting while RdData is resetting it.

TITLE	Serial Receiver, 8N1		
COMPANY	HCStronics		
DESIGNER	Bill Shen		
NUMBER	1.00	REV	A
DATE	Sun Jun 24 15:49:51 2018	SHEET 1	OF 1