Address	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00			
0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RAM start		
BFFF	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	RAM end		`!(A14 & A15) = RAM`
C000	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IO Start		`(A14 & A15) & !(A13 | A12) = IO`
CFFF	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	IO End		`(A14 & A15) & (A13 | A12) = ROM`
D000	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	ROM Start		NAND with bank zero signal for CS
FFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ROM End		