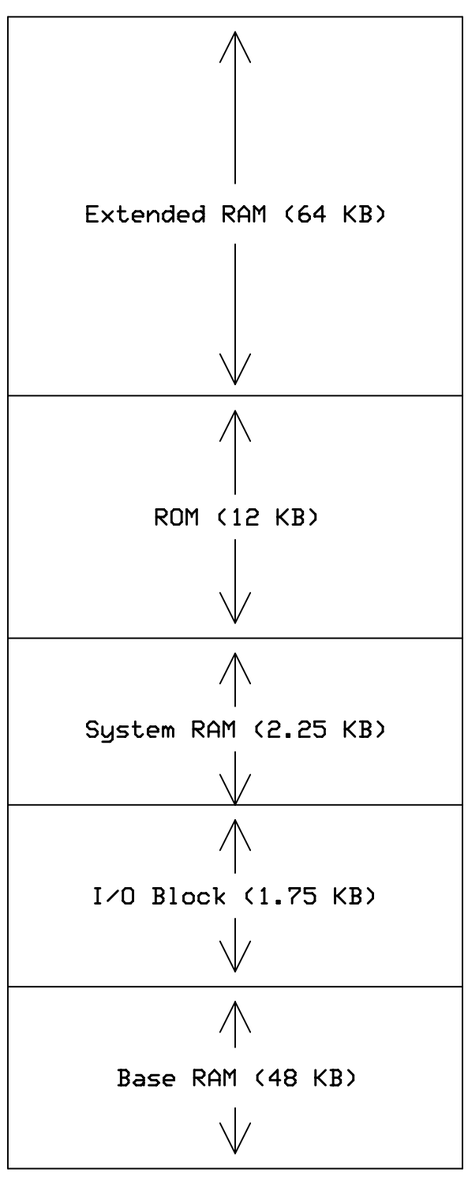
PROOF OF CONCEPT V2

SINGLE-BOARD COMPUTER

128 Kilobyte Static RAM System

Powered by the W65C816S Microprocessor

Designed by BigDumbDinosaur

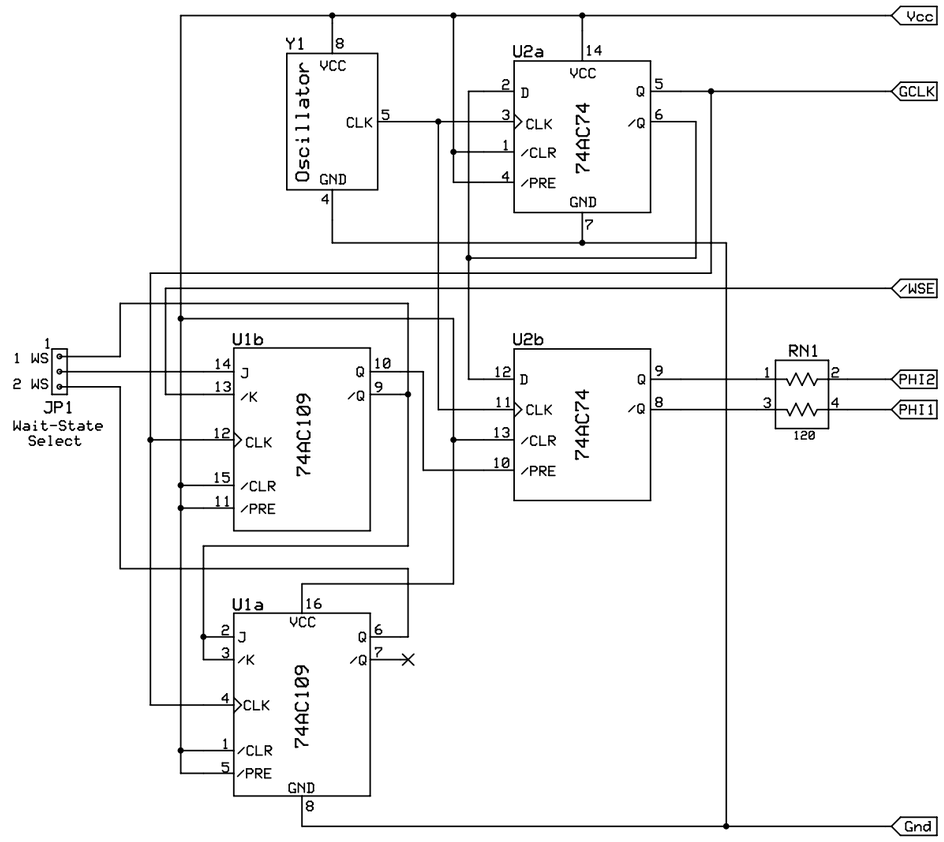

$07FFFF
Extended RAM (64 KB)
$010000
ROM (12 KB)
$00D000
System RAM (2.25 KB)
$00C700
I/O Block (1.75 KB)
$00C000
Base RAM (48 KB)
$000000

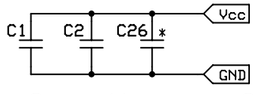
POC V2.0 MEMORY MAP

ADDRESS	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	SYMBOL	ASSIGNMENT	SIZE KB
$000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BASRAM	Base RAM Start	48.00
$00BFFF	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1		Base RAM End	
$00C000	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IOBLK	I/O Start	1.75
$00C6FF	0	1	1	0	0	0	1	1	0	1	1	1	1	1	1	1	1		I/O End	
$00C700	0	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	SYSRAM	System RAM Start	2.25
$00CFFF	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1		System RAM End	
$00D000	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	ROM	ROM Start	12.00
$00FFFF	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		ROM End	
$010000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EXRAM	Extended RAM Start	64.00
$01FFFF	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		Extended RAM End	

I/O BLOCK DECODING

	8	4	2	1	0	0	0	0		
	0	0	0	0	8	4	2	1		
	0	0	0	0	0	0	0	0		
	0	0	0	0	0	0	0	0		
ADDRESS	A15	A14	A13	A12	A11	A10	A9	A8	ASSIGNMENT	SYMBOL
$00C000	1	1	0	0	0	0	0	0	DUART #1 (chans A-B)	SIOA
$00C100	1	1	0	0	0	0	0	1	DUART #2 (chans C-D)	SIOB
$00C200	1	1	0	0	0	0	1	0	vQUART Channel IRQ Status	SIOQ
$00C300	1	1	0	0	0	0	1	1	Expansion Select A	XIOA
$00C400	1	1	0	0	0	1	0	0	Expansion Select B	XIOB
$00C500	1	1	0	0	0	1	0	1	Expansion Select C	XIOC
$00C600	1	1	0	0	0	1	1	0	Expansion Select D	XIOD





Decoupling Capacitors -- 0.1 uf @ 50v

*C26 -> Y1

CLOCK GENERATOR

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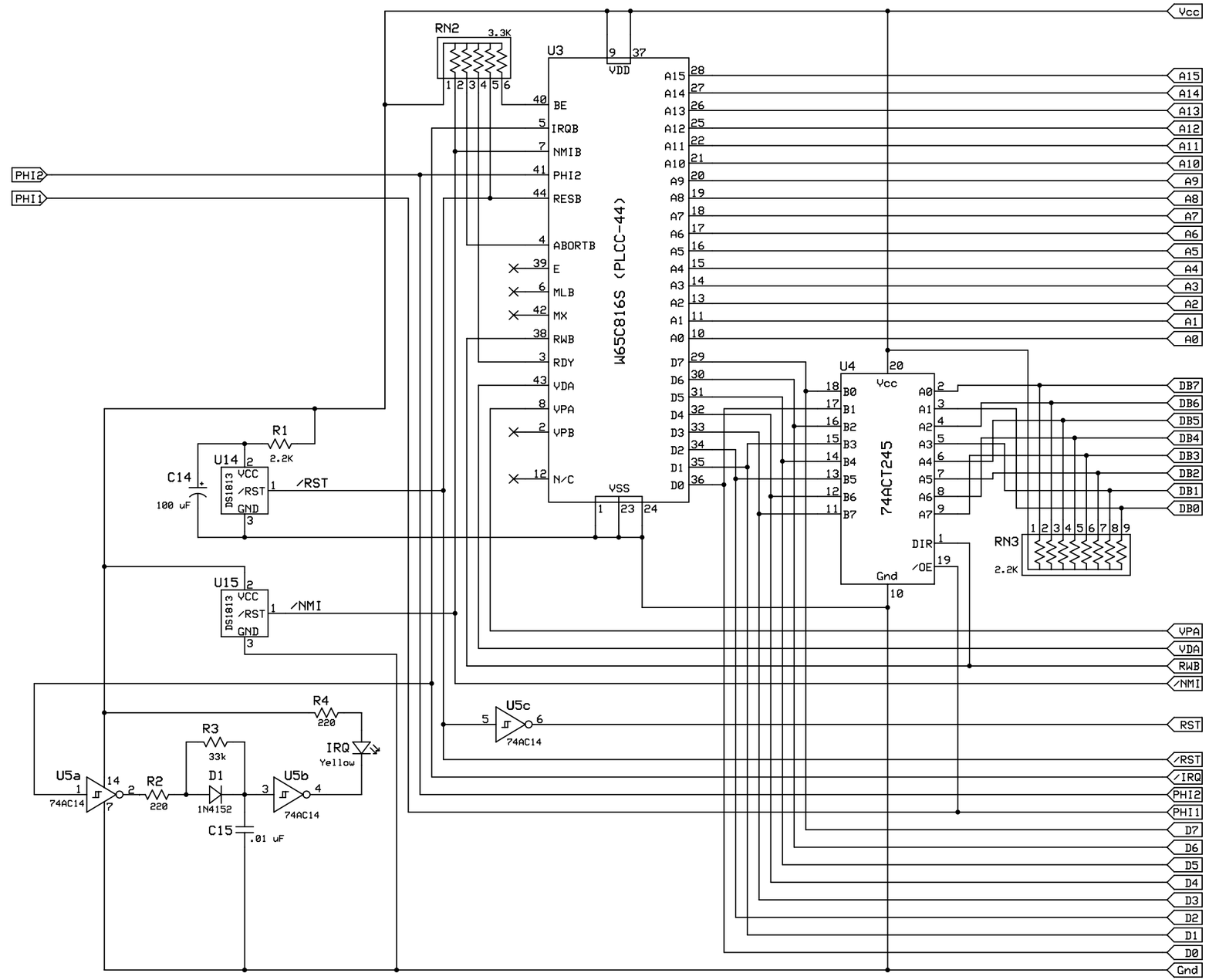

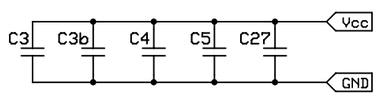

Decoupling Capacitors -- 0.1 uf @ 50v

*C27 → RN3

MPU INTERFACE

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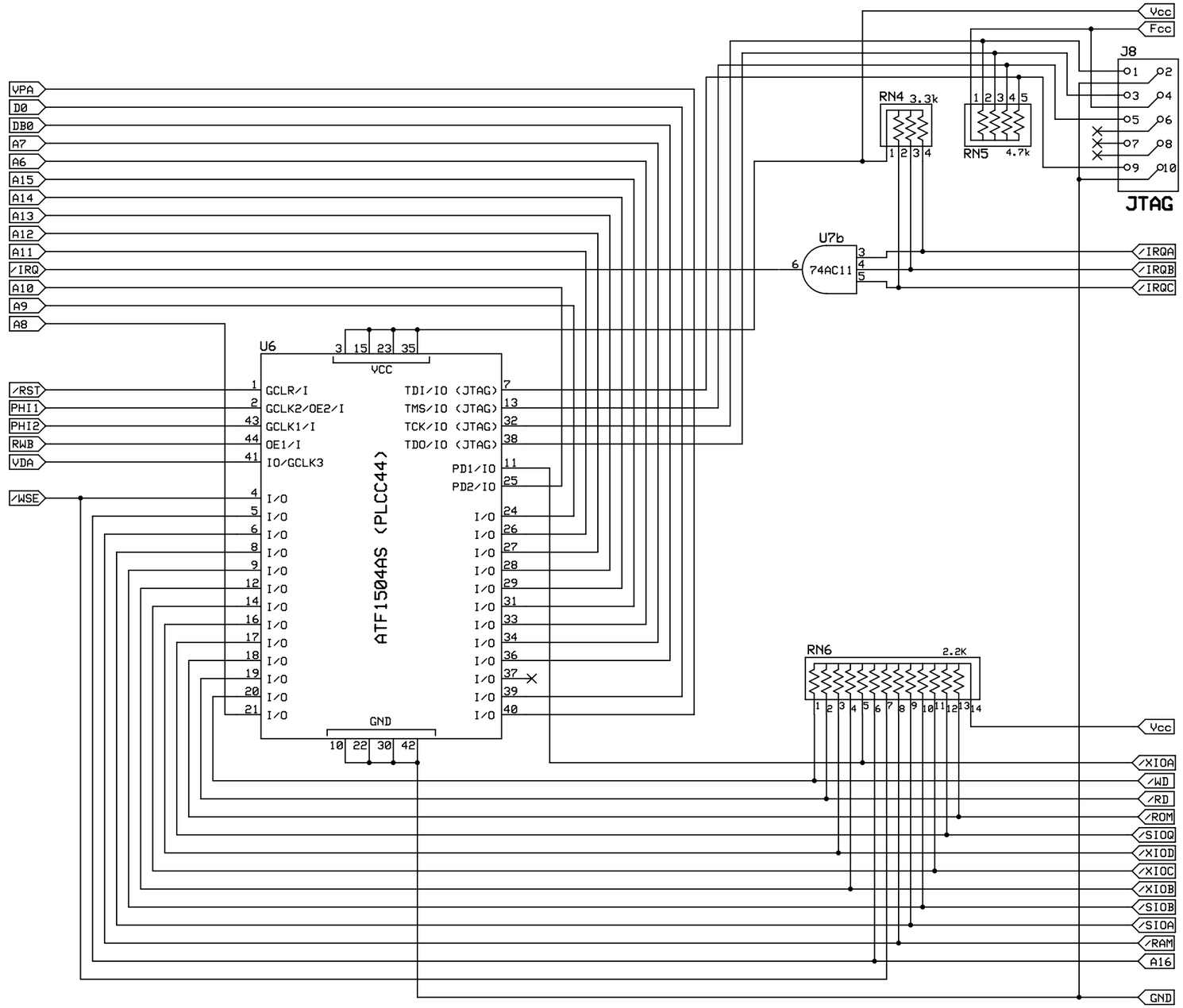

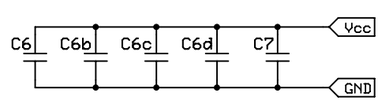

Decoupling Capacitors -- 0.1 uf @ 50v

GLUE LOGIC

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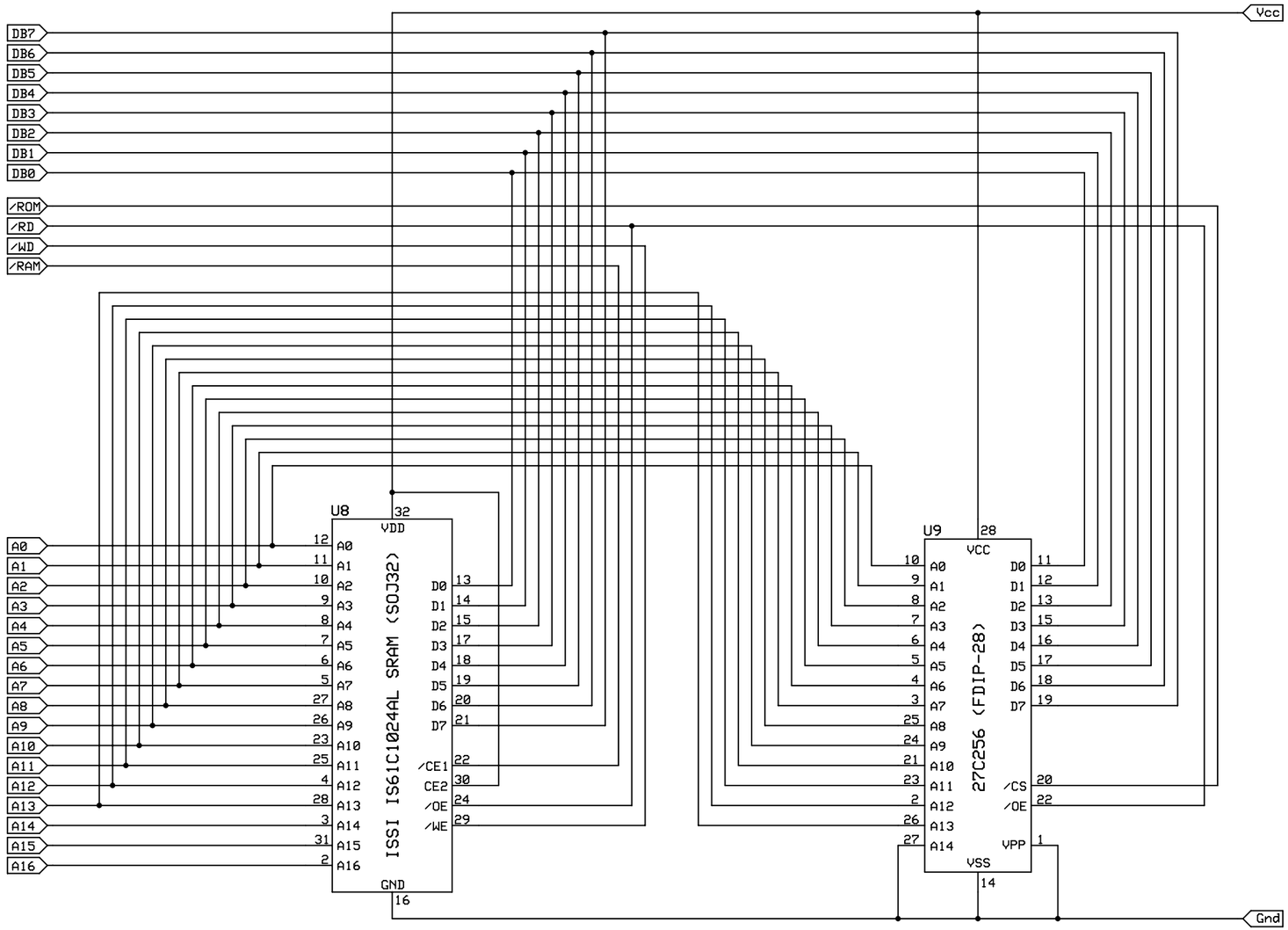

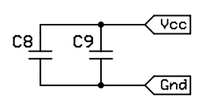

Decoupling Capacitors -- 0.1 uf @ 50v

RAM & ROM

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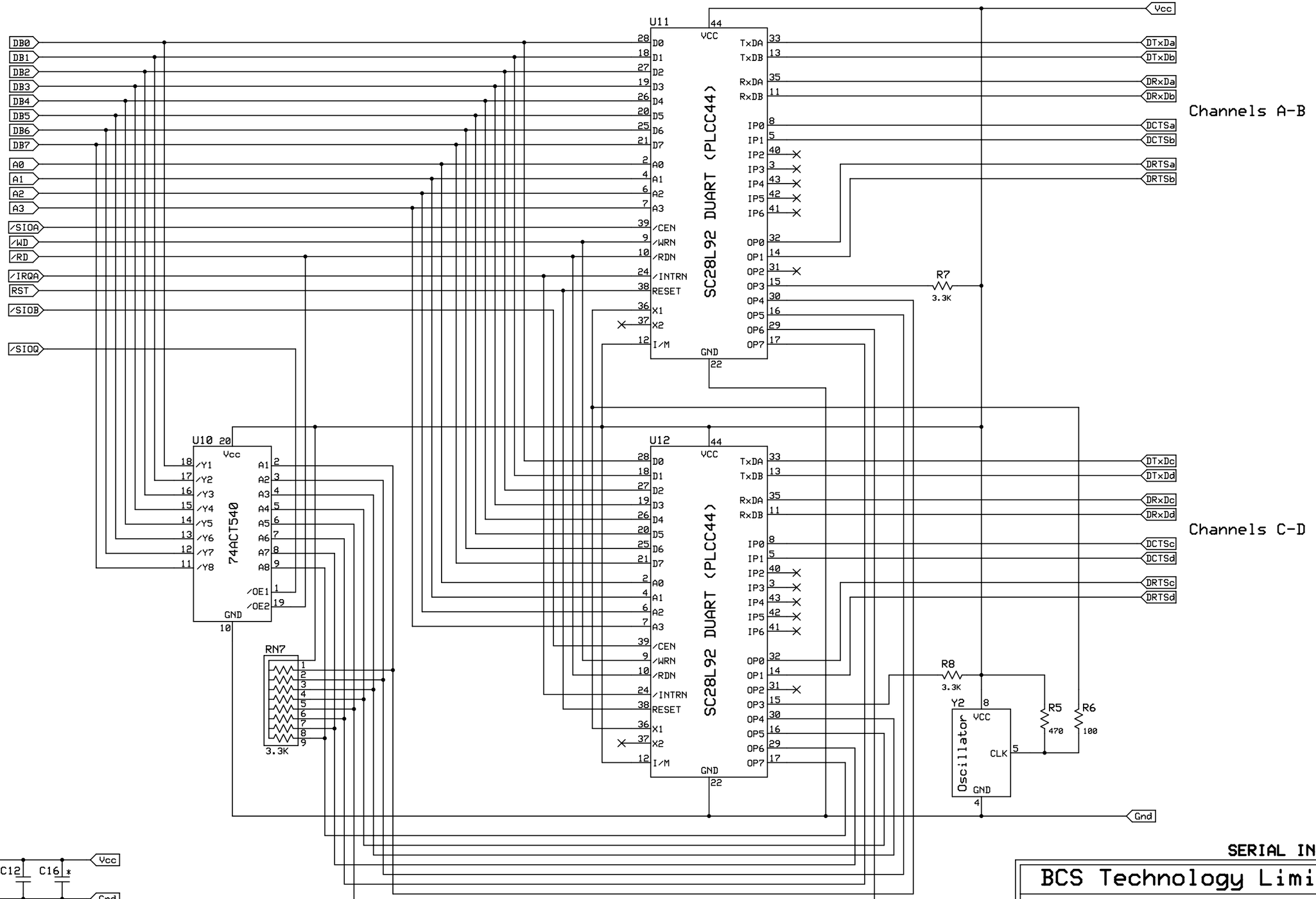
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
A0
A1
A2
A3
/SIOA
/WD
/RD
/IRQA
RST
/SIOB
/SIOQ
U11
SC28L92 DUART (PLCC44)
VCC
GND
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
/CEN
/WRN
/RDN
/INTRN
RESET
X1
X2
I/M
TxDA
TxDB
RxDA
RxDB
IP0
IP1
IP2
IP3
IP4
IP5
IP6
OP0
OP1
OP2
OP3
OP4
OP5
OP6
OP7
Vcc
DTxDa
DTxDb
DRxDa
DRxDb
DCTSa
DCTSb
DRTSa
DRTSb
Channels A-B
R7
3.3K
U10
74ACT540
/Y1
/Y2
/Y3
/Y4
/Y5
/Y6
/Y7
/Y8
A1
A2
A3
A4
A5
A6
A7
A8
/OE1
/OE2
U12
DTxDc
DTxDd
DRxDc
DRxDd
DCTSc
DCTSd
DRTSc
DRTSd
Channels C-D
RN7
3.3K
R8
3.3K
Y2
Oscillator
CLK
R5
470
R6
100
Gnd
C10
C11
C12
C16 *
Decoupling Capacitors -- 0.1 uf @ 50v
*C16 -> Y2
SERIAL INTERFACE
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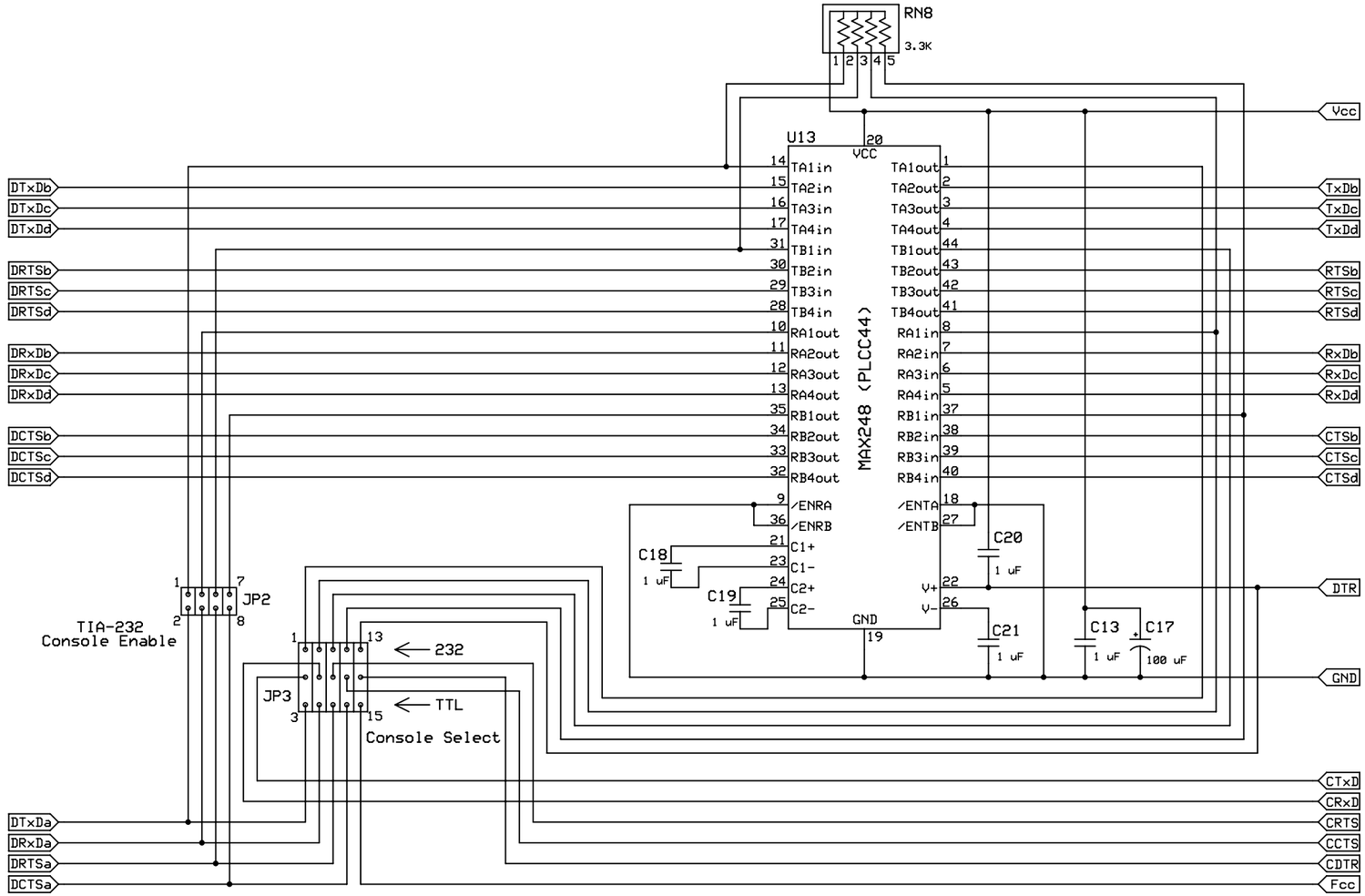

Place C13 & C17 as close to U13 as possible.

TIA232 INPUT/OUTPUT

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EXPANSION

J5

2	4	6	8	10	12	14	16	18	20	22	24	26	28	30	32	34	36		
1	3	5	7	9	11	13	15	17	19	21	23	25	27	29	31	33	35		

Vcc
Gnd
Fcc
/XIOA
/XIOB
/XIOC
/XIOD
GCLK
PHI2
/IRQC
PHI1
/IRQB
RWB
/RD
/WD
RST
/RST
A6
A5
A4
A3
A2
A1
A0
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0

1	Ground	19	Ground
2	+5 volts DC	20	A6
3	XIOA	21	A5
4	XIOB	22	A4
5	XIOC	23	A3
6	XIOD	24	A2
7	Global clock	25	A1
8	Ø2 clock	26	A0
9	IRQC	27	DB7
10	Ø1 clock	28	DB7
11	IRQB	29	DB5
12	RWB	30	DB4
13	/RD	31	DB3
14	/WD	32	DB2
15	RST	33	DB1
16	/RST	34	DB0
17	Ground	35	Ground
18	+5 volts DC	36	+5 volts DC

F1
200 mA

C22
100 uF

C23
0.1 uF

R9
330

PG
Green

R10
330

RST
Red

C24
100 uF

C25
0.1 uF

J1

5.0 VDC
Power In

Place C24 & C25 as close to J1 as possible.

J2

CRTS
CDTR
CRxD
CTxD
CCTS

TIA-232/TTL
Console
(DTE)

RTSb
DTR
RxDb
TxDb
CTSb

TIA-232
Channel B
(DTE)

RTSc
DTR
RxDc
TxDc
CTSc

TIA-232
Channel C
(DTE)

RTSd
DTR
RxDd
TxDd
CTSd

TIA-232
Channel D
(DTE)

/NMI
PB2

J4

NMI

/RST
PB1

J3

Reset

TP1

GCLK
PHI2
PHI1

Clock Test Point

TP2

D0
D1
D2
D3
D4
D5
D6
D7

Data Bus
Test Point

CTS
GND
TxD
GND
RxD
DTR
RTS

1 2 3 4 5 6 7 8

8P8C Jack

TIA-232 Channels

EXTERNAL INTERFACE

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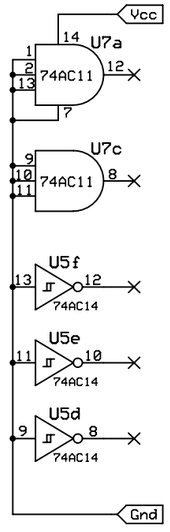

SPARE GATES

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