SECTION X

COMPUTER GRAPHICS AND RAM-DACs

COMPUTER GRAPHICS AND RAM-DACS

10

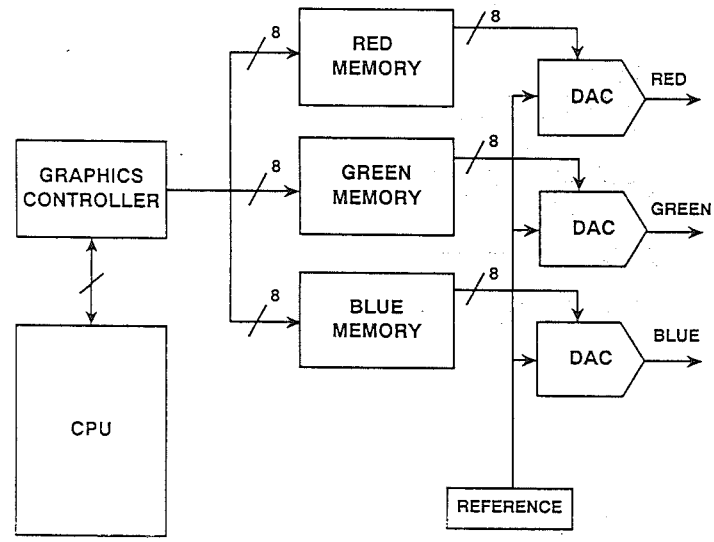
INTRODUCTION

Just as advances in microprocessor technology have been able to bring the processing power of a mainframe to desktop and laptop computers, the advances made in digital-to-analog converters have increased the performance and integration to a point where photorealistic rendering is now becoming commonplace on PCs. The drive towards larger displays, windows based graphics systems, higher resolution, and lower cost is expanding the options available to designers. This section deals with Video DACs and RAM-DACS and methods to enhance computer graphics systems.

COMPUTER COLOR GRAPHICS SYSTEMS

There are several system architectures which may be used to build a graphics system. The most general approach is illustrated in Figure 10.1. It consists of the host microprocessor, a graphics controller, three color memory banks or frame buffer, one for each of the primary colors red, green and blue (only one for monochrome systems), three high speed video DACs (only one for monochrome), and a voltage reference. The microprocessor provides the image information to the graphics controller. This information typically includes position and color information. The graphics controller is responsible for interpreting this information and adding the required output signals such as sync, blank, and memory management tasks. The memory holds the intensity information for each pixel on the screen. The DACs use the words in the memory and information from the memory controller to write the pixel information to the monitor. The reference provides a stable voltage to the DACs.

This system, when used with 8 bits for each DAC, is known as a 24 bit true color system. A total of 16.8 million addressable colors can be displayed simultaneously. The system is straightforward, but is very memory and bus intensive since each DAC must have a frame buffer associated with it. The memory requirements are based on the CRT resolution and is equal to the number of horizontal pixels times the number of vertical pixels. For an 800 x 600 Enhanced VGA display, this requires 480,000 bytes per DAC. The price of photorealistic rendering is even higher at over 4MB per DAC.



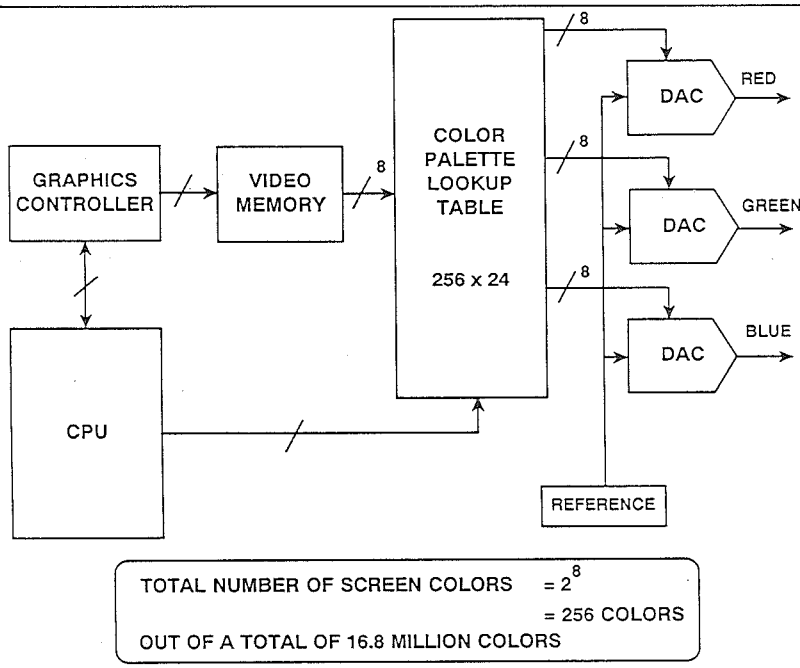
TRUE COLOR 24-BIT RGB GRAPHICS SYSTEM

Figure 10.1

COLOR LOOK-UP TABLES

In an effort to reduce system costs while maintaining a high degree of flexibility, an alternative configuration was developed. Known as a pseudo-color system, the architecture shown in Figure 10.2 reduces memory requirements to 1/3 of the true color system.

The color look-up table (CLUT) allows a total of 2^N simultaneously displayed colors to be used out of a total of 2^{M*3} available colors, where N is the number of address bits of the CLUT and M is the number of bits of each DAC. For an 8 bit VGA pseudo-color system, 256 colors may be displayed on the screen at once selected from a palette of 16.8 million colors. For the majority of business and home applications, this is sufficient.



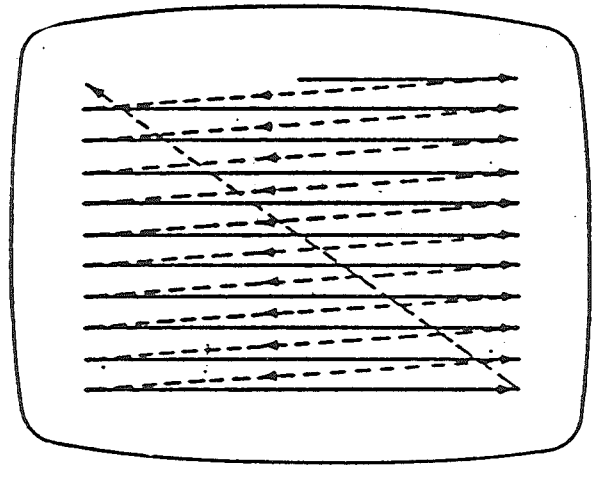
PSEUDO COLOR 8-BIT RGB GRAPHICS SYSTEM
Figure 10.2

VIDEO FORMATS

Standard computer graphics monitors, like television monitors, use a display technique known as raster scan. This technique writes information to the screen line by line, left to right, top to bottom as shown in Figure 10.3. The monitor must receive a great deal of information to display a complete picture. Not only must the intensive information for each pixel be present in the signal, but information must be provided to determine when a new line needs to start (HSYNC) and when a new picture frame should start (VSYNC). The computer industry has generally standardized around EIA standard RS-343A.

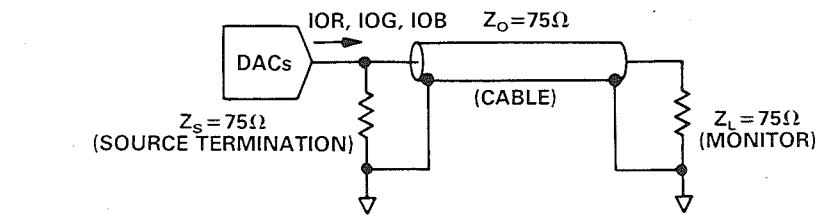
Figure 10.4 shows the RS-343A voltage standard. There are three regions within the signal, Sync, Setup and Intensity. Three signals are required by a color monitor to drive the Red, Blue and Green guns. However most monitors only require that the sync signal be present on the Green signal. Peak to peak signal levels on the green signal are 140 IRE units within the region between the blank and the reference white levels of the signal. The red and blue peak signals have 100 IRE units or 0.714 Volts, lower than green because there is no sync info.

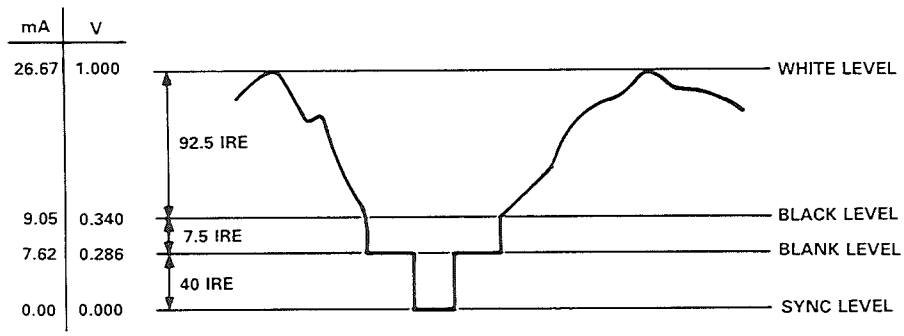
The sync region is defined as having 0.286V ± 0.05V or 40 IRE units. This portion of the signal tells the monitor when to retrace horizontally and vertically. The setup region is between the blank and black levels and has 0.054V ± 0.018V or 7.5 ± 2.5 IRE units. This portion turns off the intensity to the guns during retrace. Blank level is below reference black to insure no writing to the screen even when the screen intensity is turned up. Finally, the intensity information consisting of 0.660V ± 0.018V or 92.5 ± 2.5 IRE units, lies between reference black and reference white levels. It is this portion of the signal which is controlled by the DAC. Thus, the maximum number of colors available is determined by the resolution of the DAC, as is illustrated by Figure 10.5.



RASTER SCAN DISPLAY

Figure 10.3





RS-343A VIDEO OUTPUT

Figure 10.4

MAXIMUM NUMBER OF AVAILABLE COLOR PALETTES

DAC BITS N	DAC OUTPUT LEVELS 2^N	AVAILABLE COLOR PALETTES 2^{3N}
1	2	8
2	4	16
3	8	512
4	16	4,096
5	32	32,768
6	64	262,144
7	128	2,097,152
8	256	16,777,216

Figure 10.5

SPECIFICATIONS

It is important to be aware of the effect of a DAC specification on display performance. Important specifications include number of bits and differential non-linearity (DNL), update rise, rise and fall times, settling time, glitch impulse energy, feedthrough rejection and drive capability.

As was shown in the previous section, the number of bits a DAC has determines the number of potentially available colors that can be displayed. This assumes that the DAC has a DNL of ±1 LSB or better. The lower the DNL, the higher the accuracy for controlling color and intensity.

The update rate is typically the gateing specification used in determining if a DAC is fast enough to be used to drive a monitor of a given resolution. Figure 10.6 shows the equation for calculating the required video DAC update rate for a non-interlaced screen. The retrace factor accounts for the fact that the display is blanked for the horizontal and vertical retrace which typically account for about 25% to 30% of a given frame time. Figure 10.7 shows the DAC update rate required for various monitor resolutions.

VIDEO DAC UPDATE RATE

DAC update rate (Hz) = (Pixels/Line) • (Lines/Frame) • (60) • 1.30

- Pixels/Line = Horizontal Resolution
- Lines/Frame = Vertical Resolution
- 1.30 = Retrace Factor
- 60 Hz = Refresh Rate

Figure 10.6

GRAPHICS RESOLUTIONS

RESOLUTION	UPDATE	APPLICATION
500 X 250	10 MHz	LOW-END PC (HOME COMPUTERS)
640 X 480	25 MHz	PC
800 X 600	38 MHz	PC
768 X 576	35 MHz	PC
1024 X 768	65 MHz	PC AND LOW-END WORKSTATIONS
1024 X 1024	85 MHz	LOW-END WORKSTATIONS
1280 X 1024	105 MHz	CAD/CAE AND WORKSTATIONS
1500 X 1024	125 MHz	3D IMAGING AND HIGH-END WORKSTATIONS
1500 X 1500	180 MHz	3D IMAGING
2048 X 2048	330 MHz	PHOTO-QUALITY

60 Hz NON-INTERLACE REFRESH RATE

Figure 10.7

The time it takes for the output of a DAC to transition from 10% to 90% of the full scale range is known as rise time (fall time is from 90% to 10%). Rise and fall times must be small for high update rate DACs. Settling time is the time it takes the output to transition from one band and settle within another band. Settling time affects the performance of a color graphics system only if it is longer than the pixel interval, in which case, depending on phosphor characteristics, colors may not be accurately rendered. Additionally, the settling time will be smaller for higher speed DACs.

Glitch impulse area was covered extensively in Section IX of this seminar. Glitching can cause the signals transmitted to the monitor to have an erroneous value, thereby causing changes in color or intensity and can even create ghosts. When trying to minimize glitching, first pick a DAC with low glitch impulse area. Second, choosing the correct logic family to control the DAC is essential. Lastly, deskewing the digital inputs and controls may be of help as was pointed out in Section IX.

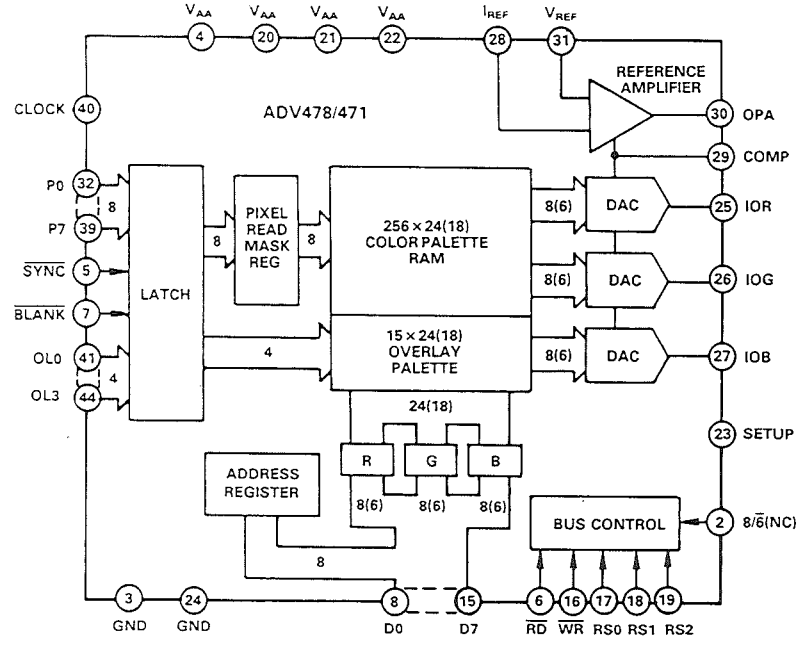
Feedthrough of either the clock or the digital data can result in noise at the output of the DAC. Feedthrough rejection tends to decrease as frequencies go higher, and therefore at high edge rates. To minimize feedthrough, use of slower speed logic can help reduce feedthrough noise, but may result in higher glitch impulse in video DACs.

In order to minimize the ghosting and distortion caused by impedance mismatch at the output, the DAC should be capable of driving a doubly terminated 75 ohm loads to RS-343A levels as shown in Figure 10.4.

RAM-DACs

The development of advanced CMOS processes has allowed the integration of the DACs, CLUT RAM, reference and logic on a single chip. Figure 10.8 shows a block diagram of the ADV478/471, pseudo-color, VGA compatible Video RAM-DACs. integrated into these devices are three DACs, color look-up table comprised of the pixel palette RAM and the overlay palette RAM, various latches, registers, control logic and a reference.

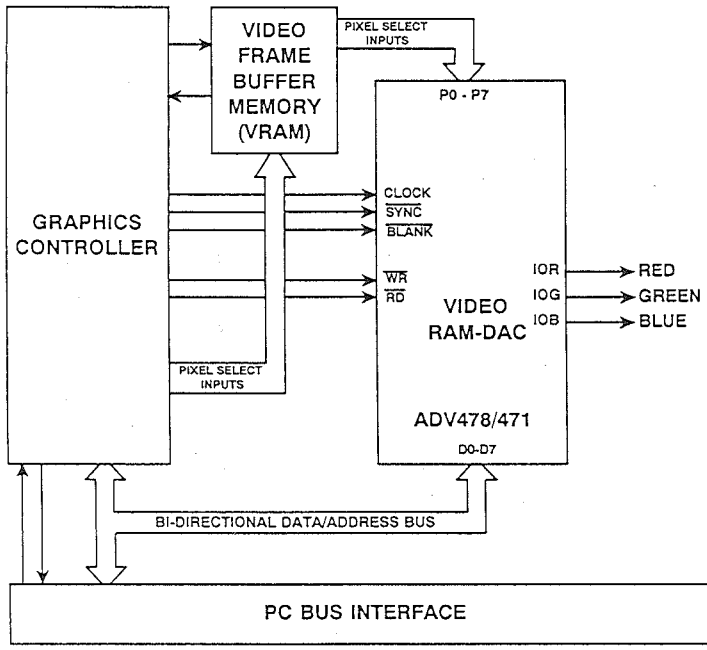
The colors associated with a particular image are loaded into the color palette RAMS through the microprocessor bus. VRAMs feed the image data into the pixel port at video rates. The pixel read mask register can be loaded through the pixel ports as well. Its function is to speed up simple animated renderings, as explained in the application note which appears at the end of this chapter. Figure 10.9 shows the architecture for the IBM PS/2 and PC VGA color graphics card. Note the component count reduction that is afforded by using RAM-DAC technology over discrete implementations shown earlier.



NOTES
1. NUMBERS IN PARENTHESIS INDICATE PIN NAMES FOR THE ADV471.
2. NC = NO CONNECT

VIDEO RAM-DAC

Figure 10.8



PS/2 & PC VGA GRAPHICS SYSTEM ARCHITECTURE

Figure 10.9

USING OVERLAY PALETTES

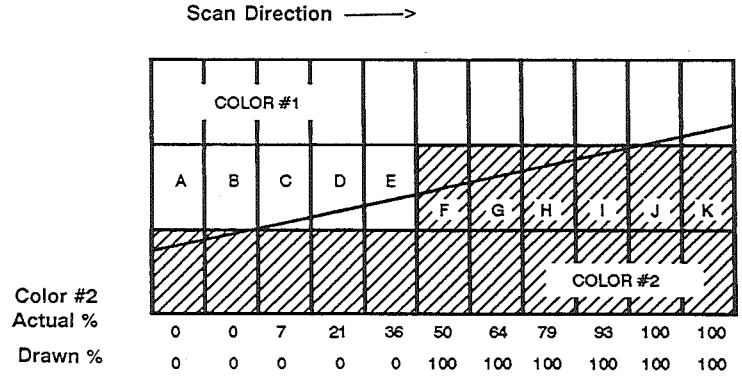
Overlay palettes are provided on RAM-DACs to reduce both hardware and software overhead when producing system level graphics shown as pull-down menus, cursors, grids, pointers, etc. The palette selection inputs control whether the pixel data will use color information from the color palette RAM or one of the overlay palettes. When at least one of the overlay bits is set high, the "Priority" overlay color addressed will be displayed instead of the color from the CLUT palettes.

By providing limited depth overlay palettes, the system software, which is generally responsible for cursor and pointer control, menus, etc., can efficiently control these graphics without altering the main graphic image which is controlled by the application software. This provides for an improvement in graphic performance, and can minimize software overhead.

By allowing independent access to the overlay palette, an EGA window may be generated over the main VGA screen image through the use of 4 bits of overlay.

CONTINUOUS EDGE GRAPHICS DIGITAL SIGNAL PROCESSOR

Graphic images of circles, lines and other objects are rendered on the monitor in a best fit method to accommodate the finite size of a pixel. A pixel is on when an object occupies 50% or more of the pixel. The pixel is off if the object crosses over less than 50% of the pixel. This graphic fact of life produces images which have jagged edges. This effect is referred to as Aliasing, and Figure 10.10 illustrates the problem. Even with a very high resolution display, the eye can quickly perceive the rough edge.

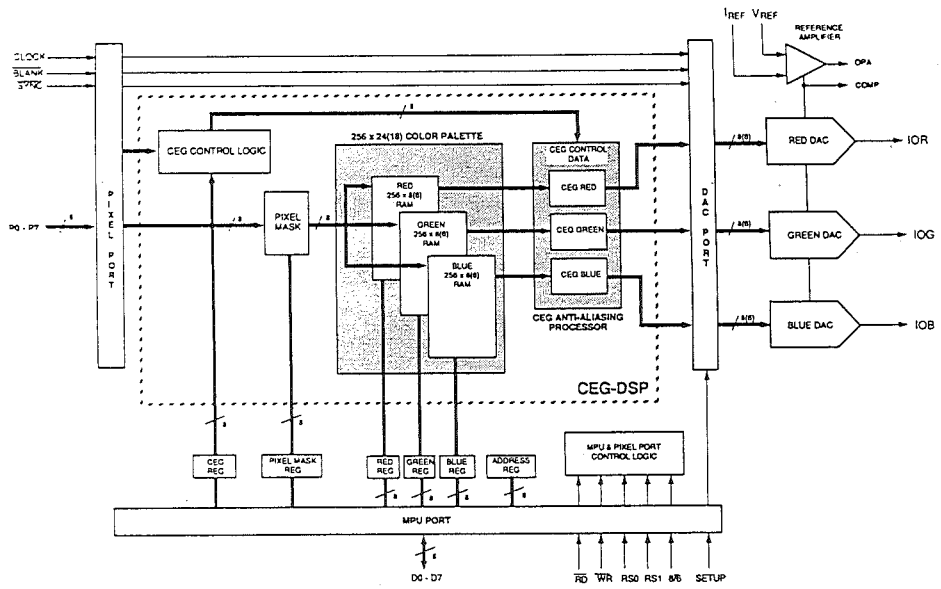


CONVENTIONAL PIXEL COVERAGE WITH ALIASING

Figure 10.10

A new device from ANALOG DEVICES dramatically improves the image quality of standard analog color systems by performing anti-aliasing and by effectively providing an extended color palette. The Continuous Edge Graphics - Digital Signal Processors (CEG-DSP) combine three matched DACs, a Color Look-up Table (CLUT), Pixel mask and a reference as shown in Figure 10.11. For designs which do not use the overlay palette, the ADV7148/ADV7141 are pin and functionally compatible with the ADV476/ADV471 and the ADV7146 is pin and functionally compatible with the ADV476 and the INMOS171/176.

The CEG achieves anti-aliasing by being able to display pixels as the linear mix of two colors from the color look-up table



CONTINUOUS EDGE GRAPHICS
DIGITAL SIGNAL PROCESSOR
Figure 10.11

(CLUT). The natural color integration of the human eye gives the display the smoothing effect as shown in Figure 10.12. When the CEG powers up, it is in a non-CEG mode, i.e., it is in a VGA compatible RAM-DAC mode. By writing a particular code sequence into the device via the MPU port, the CEG mode may be activated. In the CEG mode, the device computes the real-time weighted average on each of the primary colors which are read out of the CLUT. This computation takes the form

$$P_{MC} = [MIX \bullet P_{N-1}] + [(1\text{-}MIX) \bullet P_N],$$

where P_{MC} = Mixed Color

P_N = New Pixel Color

P_{N-1} = Previous Pixel Color

MIX = Ratio of Previous Color to New Color

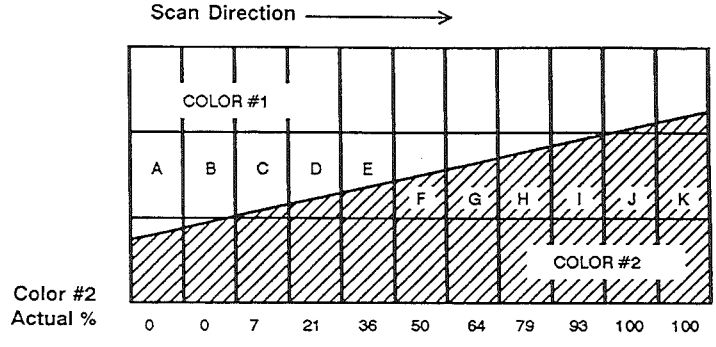
or alternatively,

Mixed color = (Ratio of the Previous Color • Previous Color) + (Ratio of the New Color • New Color).

These mixed colors, one per DAC (Red, Green, Blue), are then input into a gamma correction circuit. The outputs then drive the three DACs.

In addition to the anti-aliasing effect the CEG provides, the linear mixing of colors effectively extends the number of simultaneously available colors. This is of particular importance to applications involving photoquality rendering and solids modeling. The blending of colors allows

for the perception of much greater depth. Mixed colors, one per DAC (Red, Green, Blue), are then input into a gamma correction circuit. The outputs then drive the three DACs.



USING CEG DSP TO ELIMINATE ALIASING

Figure 10.12

VIDEO DAC SELECTION GUIDE

MODEL	RESOLUTION	UPDATE RATE	COMMENTS
AD9702	4 BITS	125 MHz	RGB Output, TTL or ECL
AD9700	8 BITS	100 MHz	ECL, Single -5.2V Supply
AD9701	8 BITS	225 MHz	ECL, Single -5.2V Supply
AD9703	8 BITS	300 MHz	ECL, Single -5.2V Supply
ADV7120	8 BITS	30, 50, 80 MHz	CMOS Triple DAC
ADV7121	10 BITS	30, 50, 80 MHz	CMOS Triple HDTV DAC, 40 Pin DIP
ADV7122	10 BITS	30, 50, 80 MHz	CMOS Triple HDTV DAC, Sync and Blanking, 44 Pin PLCC

Figure 10.13

RAM-DAC SELECTION GUIDE

MODEL	RESOLUTION	UPDATE RATE	COMMENTS
ADV471	6 BITS	35, 50, 80 MHz	CMOS Triple Color Palette RAM-DAC
ADV478	8 BITS	35, 50, 80 MHz	CMOS Triple Color Palette RAM-DAC
ADV453	8 BITS	40, 60 MHz	CMOS Triple Color Palette RAM-DAC
ADV476	6 BITS	35, 50, 66 MHz	CMOS Triple Color Palette RAM-DAC. Plug-in Replacement for INMOS 171/176
ADV7150	10 BITS	85, 110, 135, 170 MHz	CMOS 24 Bit True Color Triple Palette RAM-DAC
ADV7151	10 BITS	85, 110, 135, 170 MHz	CMOS Pseudo Color Triple Palette RAM-DAC
ADV7148	8 BITS	35, 50, 66 MHz	CMOS CEG DSP Triple Palette RAM-DAC
ADV7141	8 BITS	35, 50, 66 MHz	CMOS CEG DSP Triple Palette RAM-DAC
ADV7146	6 BITS	35, 50, 66 MHz	CMOS CEG DSP Triple Palette RAM-DAC. Plug-in Replacement for INMOS 171/176

Figure 10.14

REFERENCES

1. W. A. Kester, "Fast DACs Aid Raster-Scan Displays", **Electronic Design**, April 30, 1981.

2. W. A. Kester, "Test Setups Judge Speed of Ultrafast 8-Bit DACs", **Electronic Design**, May 14, 1981.

3. W. A. Kester, "Design of Raster Scan Graphics Systems", **Digital Design**, August 1982.

4. Tom Tice, "8-Bit, 300 MHz Monolithic D/A Converter for Displays", **Analog Dialogue**, 21-1, 1987.

5. Margery S. Conner, "Color-Palette Chips Bundle Extra Features with RAM Lookup Table and DACs", **EDN**, Sept. 29, 1988, pp. 67-76.

6. Bill Slattery and John Wynne, "Design and Layout of a Video Graphics System for Reduced EMI", Analog Devices, E1309-15-10/89, Included in this Section.

7. Bill Slattery and Eamonn Gormley, "Animation Using the Pixel Read Mask Register of the ADV47X Series of Video RAM-DACs", Analog Devices, E1316-15-10/89, Included in this Section.

ANALOG DEVICES

APPLICATION NOTE

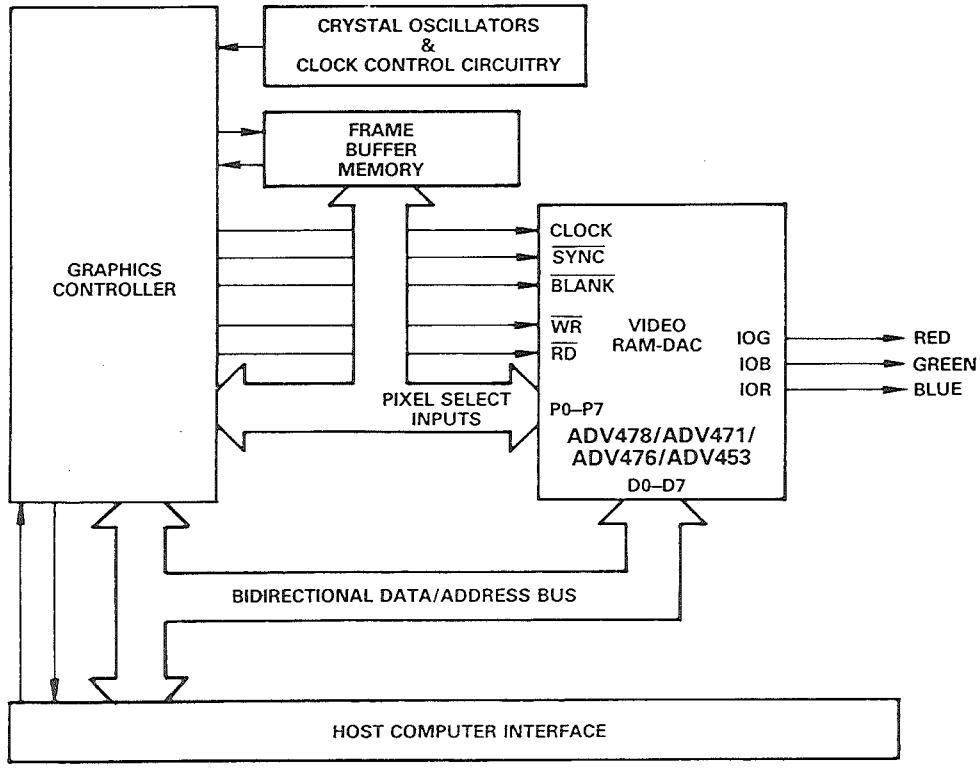
ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

Design and Layout of a Video Graphics System for Reduced EMI

by Bill Slattery & John Wynne

The availability of low cost, high performance video RAM-DACs is a key element in the spread of personal computers into application areas previously considered the preserve of expensive, high-end computer systems. Applications such as Computer Aided Engineering (CAE), Computer Aided Design (CAD), Solids Modelling, Desktop Publishing, etc., are becoming more widespread as the cost of the necessary hardware drops. Successfully incorporating a video RAM-DAC into a personal computer or onto a video graphics plug-in board is not difficult once some basic concepts are grasped and some simple guidelines followed.

This application note is intended as a guide to the design of a video graphics system in terms of Electromagnetic Compatibility (EMC). EMC design will be considered as the technique of reducing radiated emissions and Electromagnetic Interference (EMI) from a high speed video graphics system. EMC implies that the system should not electrically or magnetically interfere with its surroundings, and conversely, the surroundings should not interfere with the operation of the system. In order to provide control of EMI in the radio spectrum, government agencies and other international organizations have established limits relating to EMI, most notably, the U.S. government's FCC Part 15.



Simplified Block Diagram of a Typical Graphics System Using a Video RAM-DAC

10

OVERVIEW

This application note is divided into a number of sections as outlined below:

1. International EMI Regulatory Bodies – guidelines, testing and radiation limits.
2. System Noise Identification – identifying various sources of noise in a system.
3. PCB Layout & Design – component placement, multilayer boards, grounding, shielding and filtering components
4. Practical example of a VGA board design and associated FCC Testing.

REGULATIONS CONTROLLING EMI

The ultimate goal which must be achieved if EMC design is to be considered successful is the attainment of "Agency Certification." A number of international government agencies impose strict criteria on the allowable electromagnetic interference that electronic apparatus can emit. Electronic apparatus is required by law to conform to these agency limits, or else face severe government penalties.

In the United States, the Federal Communications Commission (FCC) is the national regulatory body which sets down strict controls on interference from computing devices. The FCC has divided computer interference into two principal types. The first type, and by far the most demanding of the two, deals with radiated emissions over the frequency range of 30 MHz to 1 GHz. Radiated emissions from personal computers, in a commercial environment, must conform to the limits set out for a Class B computing device pursuant to Subpart J of Part 15 of the FCC Rules. Table I lists the maximum permissible radiation from such devices, measured in terms of Electric Field Strength.

Frequency MHz	Distance Meters	Field Strength* μV/Meter
30–88	3	100
88–216	3	150
216–1000	3	200

Table I. Radiation Limits for Class B Computing Devices According to FCC Rules

The second type of emission deals with interference fed back onto the power lines. The FCC conduction limit on this interference is 250 μV* maximum over the frequency range 450 kHz to 30 MHz. This type of interference is heavily influenced by the design of the switched-mode power supply within the computer cabinet.

FCC Certification is awarded on the submission to the FCC of a complete report which consists of acceptable test results as well as a detailed description of the test and measurement procedure. Testing has to be carried out by an FCC-accredited test laboratory.

Class C Certification, which has less stringent limits, is allowable in certain commercial and industrial applications.

A list of the various international agencies is given in the Reference section. All agencies have very similar requirements to those of the FCC.

NOISE SOURCES

Identification of noise sources or potential noise sources in a system is the first and probably the most valuable step that has to be taken for successful EMI design.

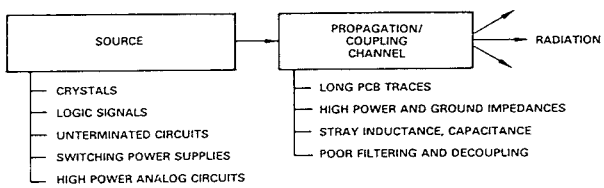


Figure 1. Noise Model of a Video Graphics System

It may even be possible to eliminate a particular noisy circuit completely from the design thus avoiding the later need for filtering. Unfortunately, many possible sources of noise cannot be eliminated from the design, but by being aware of their existence, their effects can be minimized at the source and in the coupling channel by optimum filtering and decoupling. Some of the inherent sources of noise in a video graphics system include:

1. Crystal oscillator and clock frequency division circuits.
2. Circuits with fast transition times (rise/fall times), e.g., logic families that are unnecessarily fast.
3. Unterminated circuits.
4. Stray inductances/capacitances.
5. Switching power supplies.
6. High power analog circuits such as video RAM-DACs.

Crystal Oscillators & Associated Circuitry

A video system usually contains a number of crystal oscillators and associated clock and pixel data circuits, which are required to achieve various on-screen pixel resolutions. In a VGA system, for example, there could be as many as five crystal oscillators varying in frequency from 25 MHz to 65 MHz, and maybe up to 80 MHz. These crystal oscillators and their associated circuitry tend to be rich in unwanted noise and harmonic components. They can be a prime source in the generation of EMI if some basic guidelines are not followed.

***Measured pursuant to §15.840 of the FCC Rules.**

Some of the important actions are:

1. Place crystal oscillator circuits as far as possible from analog circuitry and video output connectors.
2. Isolate power supply to crystals through the use of ferrite beads.
3. Avoid the mixing of clock buffers and other logic in the same IC package.
4. Use several low power data drivers or buffers for clock and pixel data lines distributed throughout the board, in preference to using a single high power driver.

With regard to the crystal oscillators themselves, the critical aspects which must be considered include the wave shape and the transition time (rise/fall time). Figure 2 is a plot of the output frequency spectrum of a typical 28.5 MHz crystal oscillator. It shows the amplitude of the harmonic components relative to the fundamental. It can be clearly seen that although the crystal's fundamental frequency lies outside the FCC's lower limit of 30 MHz, for radiated EMI, higher-order harmonic components exist throughout the FCC-controlled band. The frequency of the crystal oscillators should be kept to the required minimum, and transition times should be kept as slow as possible. This reduces the amplitude of unwanted harmonics, while still satisfying system functional performance needs.

The clock circuitry, which includes crystal oscillators and pixel data lines, is the primary source of most of a system's noise. Keeping this circuitry as far and as isolated as possible from other circuitry, especially analog circuitry, is all-important. On the other hand, it could be argued that by running long pixel data and clock lines from such circuitry to the Video RAM-DAC in itself is not desirable. Long lines increase noise coupling to other parts of the system. A tradeoff between length of pixel lines and the placement of high speed clock circuitry must be considered. The designer must attempt to optimize these two competing goals. As was mentioned earlier, the use of multiple low power buffers will help to ease such a conflict. A distance of less that three inches between buffers would be desirable in such circumstances.

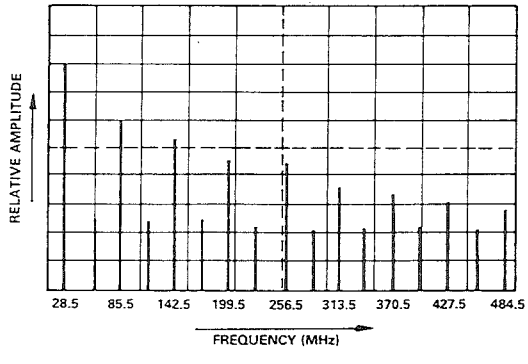


Figure 2. Magnitude of Harmonic Components Relative to the Fundamental for a 28.5 MHz Crystal Oscillator

Other Noise Sources

A number of other noise generators can be easily identified. Circuits with fast transition times including memory chips, logic circuitry and the graphics controller all contribute to the overall noise of the system. The faster the signal transition time, the greater will be the amplitude of the resulting harmonics, as was seen in the previous section relating to crystal oscillator circuits.

As a general rule, devices with the slowest possible rise/fall times that will achieve the system's tasks should be used. Table II lists some typical rise/fall times for various logic families.

Technology	IC Family	Transition Time
TTL	74	10 ns
	74LS	12 ns
	74ALS	3→20 ns
	74S	6 ns
	74AS	2→9 ns
	74F	1.2→8 ns
CMOS	74HC	20→150 ns

Table II. Comparison of Transition Times for IC Logic Families

Stray inductances and capacitances can cause signals to ring, to overshoot or undershoot the steady state voltage levels. This ringing is a source of EMI which can be minimized by keeping wires or traces short and adding series, damping resistances at the source or termination of long signal paths.

Unterminated circuits with floating signal lines should be avoided. Unwanted oscillations can result.

Power to all devices of a system is usually derived from switch-mode power supplies. While the design of the power supply is critical to the reduction of conducted noise in the FCC's band of 450 kHz up to 30 MHz, harmonics generated by the switching power supplies can extend well into the radiation frequency band and thus add to EMI.

Modern high resolution color graphics monitors are driven by analog signal levels direct from the DACs. The relatively high power, analog output levels from the Red, Green and Blue current sources of the video DAC require careful attention. As will be discussed in the PCB layout section, the power to the Video RAM-DAC should be isolated from the remainder of the PCB power plane. If noise on the high speed pixel and clock input section to the Video RAM-DAC has not been minimized, noise will be coupled through to the analog output section and onto the connecting cable to the monitor, causing this cable to act as an antenna. Filtering at the source termination of each of the three DAC outputs can be used if required to minimize the noise further. (See Appendix 1, *Three-Terminal Capacitor.*)

PRINTED CIRCUIT BOARD DESIGN

The extent of radiated emissions from a printed circuit board (PCB), will be determined by the effectiveness of the PCB to act as a propagation channel for unavoidable noise sources, its ability to couple this noise onto other circuitry, and the radiation into free space of this undesired noise. Apart altogether from a PCB's ability to radiate EMI, noise coupled from digital circuits on the board to the video RAM-DAC can adversely affect the system's functional performance.

Causes of EMI

The main sources which conduct or radiate EMI from a printed circuit board are as follows:

1. Common impedance coupling via power and ground traces.
2. Antenna loops formed by ICs and their bypass capacitors. Note that these loops also include the power and ground lead frame members within the IC packages.
3. Printed circuit board traces carrying signal currents. Note again that signal lead frame members within the IC packages are also included.
4. Crosstalk between adjoining signal traces.

Common Impedance Coupling

An example of common impedance coupling via power and ground traces is shown in Figure 3a where a number of logic gates are supplied with power over common printed circuit board traces. A typical V_{IN} input signal to one of these gates is shown in Figure 3b with the resulting transient and signal currents due to the gate switching also shown.

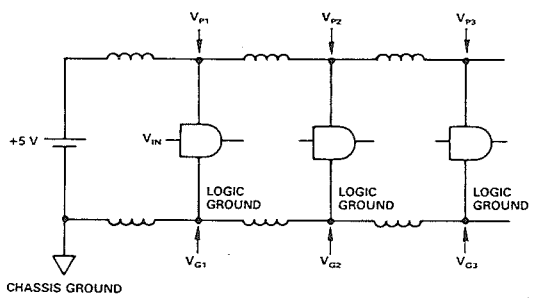


Figure 3a. Common Impedance Coupling via Power and Ground Traces

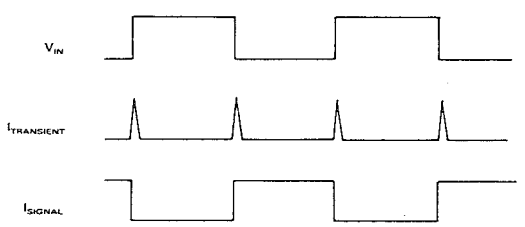


Figure 3b. Signal and Transient Currents Due to Gate Switching

The distributed trace inductances act as impedances to these switching currents spreading the resulting high frequency noise to all nodes common to the culprit. To get an idea of the magnitude of the generated high frequency noise, let's take a look at the effect of a single gate, as shown in Figure 4a. The associated worst signal current for a standard TTL gate is shown in Figure 4b.

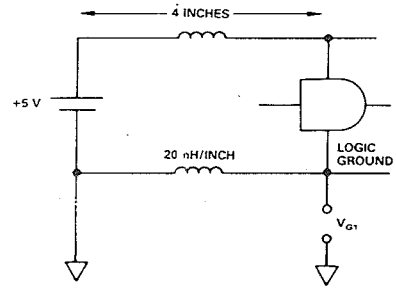


Figure 4a. Common Impedance Coupling Due to One Gate

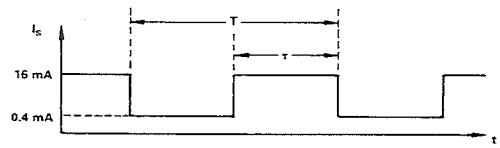


Figure 4b. Signal Current Due to TTL Gate Switching

Consider the harmonic components present in the switching signal current of Figure 4b. This assumes the gate is driving 10 standard TTL loads with a maximum sink current of 16 mA and a maximum source current of 0.4 mA.

With a mark/space ratio of τ/T and using a Fourier Series expansion, the formula for the amplitude of the nth harmonic is given by

$$I_n = \frac{2A\tau}{T}\left[\frac{Sin\left(\frac{n\pi\tau}{T}\right)}{\frac{n\pi\tau}{T}}\right]$$

where n = 1, 2, 3 . . . .

For a square wave $\tau/T = 0.5$, the amplitude of the third harmonic (n=3) is

I_3= 3.4 mA, zero to peak.

At 28.5 MHz, a standard VGA pixel clock frequency, the magnitude of the impedance of the ground trace in Figure 4a is given by

$$Z = [2\pi fL]$$

where f = 28.5 MHz
L = 20 nH/inch (typically)

hence Z = 3.58 Ω/inch.

At 85.5 MHz (3×28.5 MHz) the impedance is 10.74 Ω/inch. Thus the high frequency voltage at the logic

ground node of the switching gate due to the third harmonic alone is equal to

$$V_{G1} = (3.4 \times 10^{-3})(4)(10.74)\ V$$

$$= 146\ mV\ peak\ at\ 85.5\ MHz.$$

This high frequency component and other similar components will be circulated around the printed circuit board via the common ground traces. It will also appear on any cable shielding attached to this common ground trace and, depending on how efficient the cable shield is as an antenna, will be radiated into free space.

Antenna Loops

One of the most important principles of PCB layout and design for noise reduction can be described by the phrase:

"Minimize Signal Loop Areas."

In most circuit designs, we tend to think of the currents we're interested in as flowing "out" of one place, "through" some other place and "to" the target point. Unfortunately however, this often leads us to neglect to consider how these currents will eventually find their way back to their source. Ground and supply voltage points are considered "equivalent," and the fact that they are parts of a network of conductors through which currents flow and develop finite voltages is often not appreciated. These voltages can radiate to cause EMI, see Figure 5.

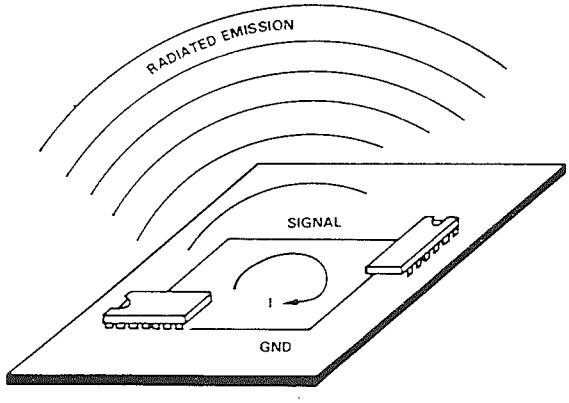


Figure 5. Currents Flowing in Large Loops Add to EMI

Voltages are generated because wires and traces do not have zero impedance due mainly to inherent inductances.

Many of the problems associated with power and ground loops can be avoided through the deployment of effective bypassing techniques.

The aim of effective bypassing is to maximize the charge stored in the bypass loop while simultaneously minimizing the inductance of this loop. Inductance in the loop acts as an impedance to high frequency transients and results in power supply spiking. Figure 6a shows a poor bypass arrangement and the associated inductances due to the large loop area are illustrated in Figure 6b.

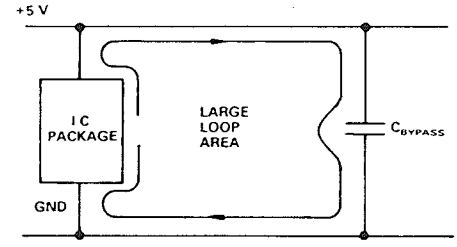


Figure 6a. Large Loop Associated with Poorly Placed Bypass Capacitor

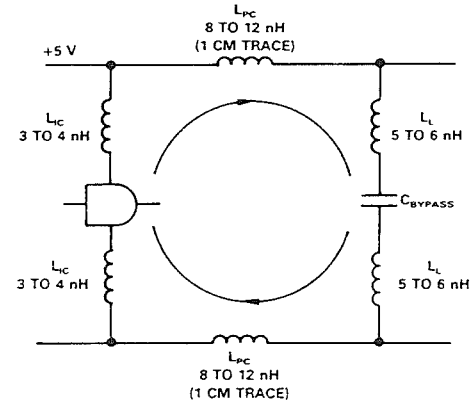


Figure 6b. Equivalent Circuit of Bypass Loop of Figure 6a

where L_L = inductance of the lead from the capacitor body to the PC board

L_{PC} = inductance of the trace between the lead arrival on the PC board and the IC pin

L_{IC} = inductance of the lead frame member carrying power within the IC package.

As well as loop inductances due to the above, the series inductance of the bypass capacitor itself must also be considered. It is well known that there is more inside a capacitor's body than a pure capacitance.

The simplified equivalent circuit of a 0.1 μF capacitor in Figure 7 shows an effective series resistance (ESR) and effective series inductance (ESL) in series with the ideal 0.1 μF capacitance.

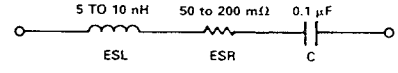


Figure 7. Equivalent Series Representation of a Bypass Capacitor

Figure 8 shows the complete inductive loop associated with the bypass circuit.

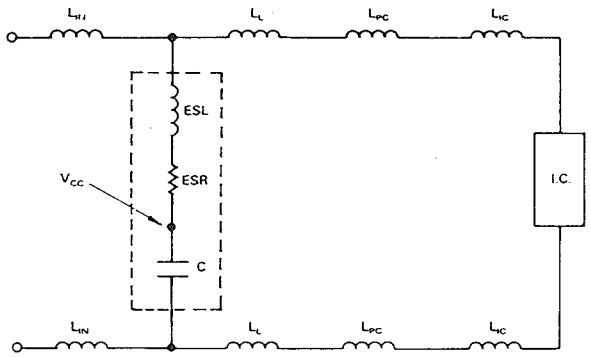


Figure 8. Inductive Loop of a Bypass Circuit

These inductances increase the total series inductance of the bypass loop and hence lower the series resonant frequency as determined by the equation:

$$fo = \frac{1}{2\pi\sqrt{LC}}$$

Above the series resonant frequency the impedance becomes more inductive, increasing linearly with increasing frequency. For instance, a 0.1 μF ceramic radial lead capacitor with 1/4 inch leads generally resonates around 10 MHz.

The minimum value of bypass capacitor required is determined by the maximum amount of voltage drop allowable across the capacitor as a result of the transient current. An approximate value for a bypass capacitor is given as

$$C = \frac{I.\Delta t}{\Delta V} \; Farads$$

where I = Maximum Transient Current
Δt = Transient Duration
ΔV = Allowable Voltage Drop.

For example, a typical 74 HC I_{CC} transient is 20 mA high lasting 20 ns. If the voltage drop is to be kept below 100 mV, then the required bypass capacitor is

(20 mA) (20 ns) / (100 mV)

or 4 nF per output.

However, any series inductance in the bypass loop will cause additional voltage spiking. For any given magnitude of noise spike, an approximate expression for the maximum amount of series inductance is given by

$$L = \frac{V.\Delta t}{\Delta I} \; Henrys$$

where V = Maximum Noise Spike
Δt = Transient Duration
ΔI = Transient Current.

The typical 74 HC I_{CC} transient of 20 mA has a rise/fall time of 4 ns. If we wish to restrict the inductive noise spike to, say, 100 mV peak, the maximum amount of series inductance is

(100 mV) (4 ns) / (20 mA)

or 20 nH.

Referring back to Figure 8, this means that the combined total of ESL, L_L, L_{PC} and L_{IC} must be kept below 20 nH. To a greater or lesser extent the first three terms are within the PC board designer's influence; the fourth term, the inductance of the IC lead frame member or L_{IC}, is invariable, being determined by the IC package. The use of PLCC packaged parts, such as the ADV478/ADV471, inherently reduces L_{IC} to 2–3 nH as against 10–12 nH for the more traditional DIP parts (see section on "Surface Mount Technology").

Appendix 1 examines in greater detail the characteristics and filtering capabilities of various bypass elements including two and three terminal capacitors.

Multilayer PC Boards

In the design of a high performance, high speed graphics system, it is recommended that a four-layer printed circuit board be used.

Figure 9 shows a cross-sectional view of a four-layer printed circuit board, with power and ground planes separating the signal-carrying traces of the component and solder sides of the PCB. As well as using multilayer boards, consideration should be given to the relevant placement of components. Figure 10 shows a suggested component placement scheme.

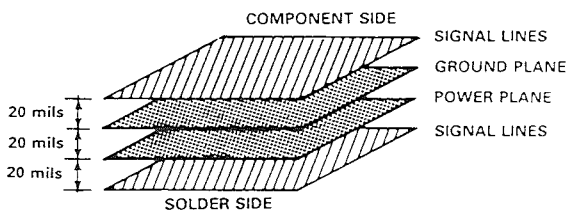


Figure 9. Four-Layer Printed Circuit Board Construction

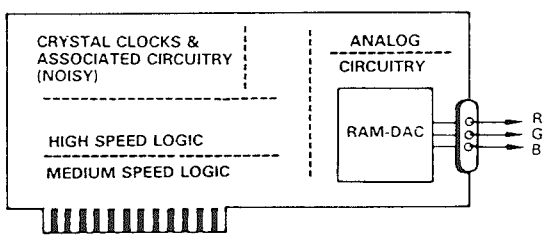


Figure 10. Printed Circuit Board Component Placement

Power and Ground Planes

Power supply decoupling attempts to contain the transient currents within the bypass loop. However it cannot be 100% successful, and some high frequency components will escape onto the power and ground traces. High frequency signal currents will also be flowing in the power and ground traces. In order to avoid common-impedance noise coupling due to these currents, it is necessary to reduce the impedance of the power and ground traces to an absolute minimum. The only satisfactory way to achieve this is not to use traces at all but to use power and ground planes. On a PC-card-sized, two-layer board with one side devoted to a ground plane, the impedance of the plane is in the tens of milliohms range.

A four-layer board allows another plane to be used as a power plane. Low impedance power and ground contacts are thus available over the full area of the board. Additionally, in a four-layer board with power and ground planes inside the board and signal traces on the top and bottom of the "sandwich," overlapping power and ground planes act as an inherent distributed capacitor, as shown in Figure 9. This provides some measure of high frequency decoupling. From the signal interconnect point of view, the major advantage of using a ground plane is the very substantial reduction in signal loop area it provides. In a typical PCB layout, signal current flows out through one trace and back through a ground trace. Such a path can include a large loop area; a large loop area, as has already been discussed, implies high inductance for the traces with follow-on consequences of signal ringing, EMI radiation and crosstalk. To reduce the inductance it is necessary to reduce the loop area through which the signal current flows. The use of power and ground planes minimizes loop areas, thereby reducing inductances and resulting EMI.

The electromagnetic fields associated with an idealized case of two parallel wires carrying equal and opposite currents are shown in Figure 11.

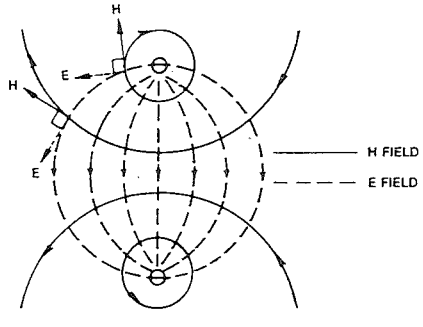


Figure 11. Electromagnetic Field about Two Parallel Conductors Carrying Equal and Opposite Currents

The two fields (electric, E, and magnetic, H) tend to be confined between or near the conductors. The electric field is strongest in the plane of the conductors. The magnetic field is nonzero at points close to the conductors, but farther away (relative to the wire spacing) the fields from both conductors tend to cancel out. Keeping the conductors together promotes field cancellation which can be viewed either as minimizing the loop area or minimizing the inductance; the results are the same.

Introducing a ground plane (sheet of copper) halfway between the wires, as shown in Figure 12, does not disturb the field pattern even when the lower wire is removed.

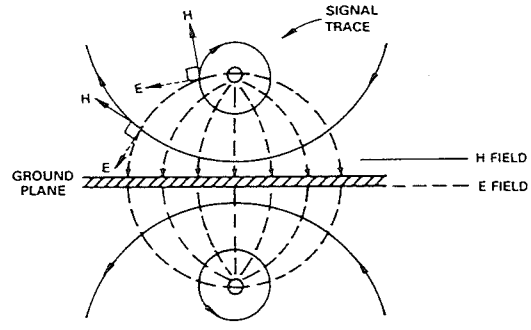


Figure 12. Electromagnetic Field about Two Parallel Conductors Separated by a Ground (Copper) Plane

A virtual image of the lower wire has been produced in the copper plane maintaining the original field configuration. This is the basis of microstrip. With a properly designed ground plane system, the return current will always flow under the signal trace, the path of lowest impedance.

Digital Signal Interconnections

The use of a ground plane allows the signal interconnects to be viewed as microstrip transmission lines whose characteristic impedances, propagation delays, etc., can be readily calculated. Microstrip is the name given to a transmission line which consists of a signal trace separated from a ground plane by a dielectric. Figure 13 shows the cross section of such a line.

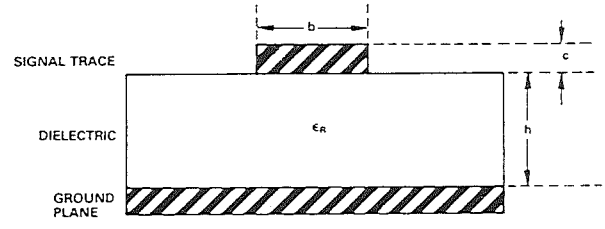


Figure 13. Cross Section of Microstrip Transmission Line

The characteristic impedance, Z_0, of this line is

$$Z_O = \frac{87}{\sqrt{\epsilon_R + 1.41}} Ln\left\{\frac{5.98\,h}{0.89\,b + c}\right\} \Omega$$

where ϵ_R = Relative Dielectric Constant of Board

typically ϵ_R = 5 for glass/epoxy boards.

b, c, h = dimensions indicated in Figure 13

The propagation delay, t_{PD}, of a microstrip line is given by

$$t_{PD} = 1.017 \sqrt{0.475 \epsilon_R + 0.67}\ ns/ft.$$

Note that this propagation delay is dependent only on the dielectric constant and not on the line geometry.

The graph below shows impedance values for various configurations of microstrip line.

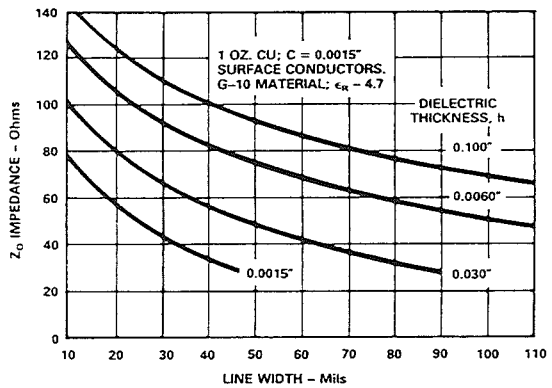


Figure 14. Impedance Versus Line Width & Dielectric Thickness for Microstrip Lines

Gross impedance mismatches between the transmission line's characteristic impedance and the source (driver output) or load (receiver input) impedances connected to the line reflect the signal back and forth on the line. These reflections will cause overshoot, EMI radiation and crosstalk. By properly terminating the line with either source or load impedances which match that of the transmission line, reflections can be eliminated or substantially reduced. However, not every signal interconnect demands line termination; the need is determined by the relationship between the rise (or fall) time of the signal and the time required for the signal to travel the length of the interconnect. As a general guideline for digital signals, line termination is needed if the one way propagation delay, t_P, over the length of the interconnect is greater than one eighth of the signal rise time, t_R, i.e., line termination is needed if

$$t_P \geq (1/8) \bullet t_R\ secs.$$

A number of dc and ac termination techniques exist which trade increased power dissipation against component count. The simplest termination technique which dissipates no extra power is a series termination one where a resistor is placed in series with the signal interconnect at the source end of the line, see Figure 15. The resistor should have a value equal to the characteristic impedance of the line minus the output impedance of the driver and should be of metal-film construction or some other low-inductance material. The load impedance is considered an open circuit. Series termination is most suitable for systems where only one receiver (e.g., ADV478/ADV471) is connected to the line. Note that if pull-up resistors are required on digital or clock signals, they should be connected to the PCB Power Plane (V_{CC}).

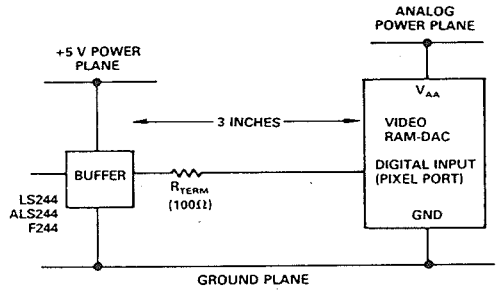


Figure 15. Series Termination of Signal Lines

Crosstalk

Crosstalk is any unwanted signal coupling between parallel PC-board traces due to mutual inductance (L_M) and capacitance (C_M), as illustrated in Figure 16.

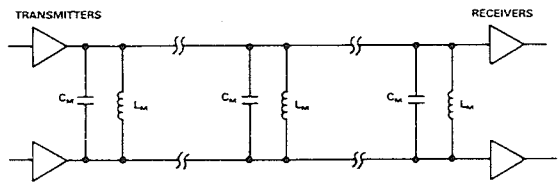


Figure 16. Capacitive and Inductive Coupling between Signal Traces

In general, crosstalk is directly proportional to line impedances, frequency and line lengths and inversely proportional to line spacing. Much of the induced crosstalk in a signal line is from immediately adjacent transmission lines which suggests that wider spacing between lines will reduce the problem. This may not always be possible in closely spaced circuits, so an alternative approach is to shield the signal lines by inserting narrow grounded traces between each signal line on the same wiring plane, as shown in Figure 17.

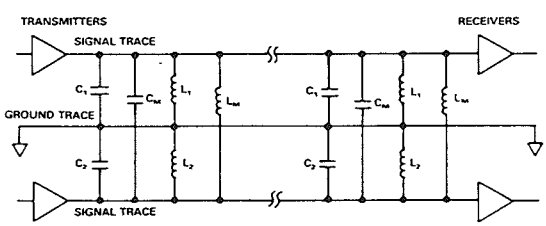


Figure 17. Ground Trace between Signal Lines Reduces Crosstalk

At high frequencies capacitive coupling dominates. The addition of a shield (or ground trace) between the signal lines changes the equivalent circuit. Crosstalk is now reduced since the inductance L_M is now much larger than either L_1 or L_2 and capacitance C_M is much smaller than either C_1 or C_2.

Separate Power Plane for Video RAM-DAC

To further isolate the Video RAM-DAC from the PCB's power supply, V_{CC}, it is recommended that a separate power plane, V_{AA}, be used for the video RAM-DAC and its associated circuitry. This analog power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a suitable filtering device such as a ferrite bead (see Appendix 1 – *Ferrite Bead Inductor*). This ferrite bead should be located no more than three inches away from the Video RAM-DAC. In the case of Analog Devices' ADV478 and ADV471, which have multiple power (V_{AA}) pins, it is important to connect all these V_{AA} pins to the analog power plane. This eliminates any possibility of latchup in the device.

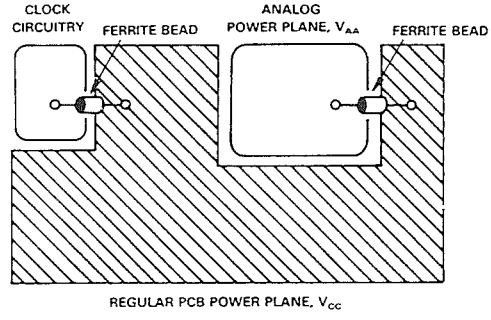


Figure 18. Power Plane Decoupling Using Ferrite Beads

Common Ground Plane

Due to the presence of RAM on board the ADV478/ADV471 and ADV476, it is not recommended to isolate the device's ground circuitry from the main PCB ground. Corruption of data could occur. These Video RAM-DACs should have all GND pins connected to the PCB's regular ground plane.

Analog Outputs

The analog outputs of Analog Devices' video RAM-DACs are driven by switched current sources. These parts are designed to drive either a singly or doubly terminated 75 Ω load. The doubly terminated configuration shown in Figure 19 is the preferred choice.

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the Video RAM-DAC be placed as close as possible to the output connector, with the analog output traces being as short as possible (less than 3 inches). The 75 Ω termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane.

As well as minimizing reflections, short analog output traces will reduce noise pick up due to neighboring digital circuitry.

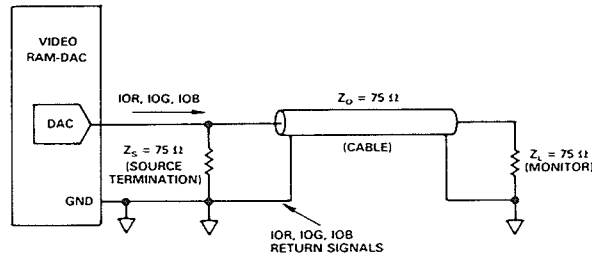


Figure 19. Recommended Analog Output Termination for Video RAM-DACs

Surface Mount Technology (SMT)

Surface mount technology (SMT) offers many EMI advantages over traditional through-hole designs. Because SMT allows the designer to place components on both sides of the printed circuit board as well as featuring smaller component sizes, it provides superior PCB integration. This means that loop lengths can be reduced and noisy signal traces can be shortened, all having a positive effect on EMI. The shorter lead lengths of SMT packages decrease inductance, thereby providing better high frequency performance.

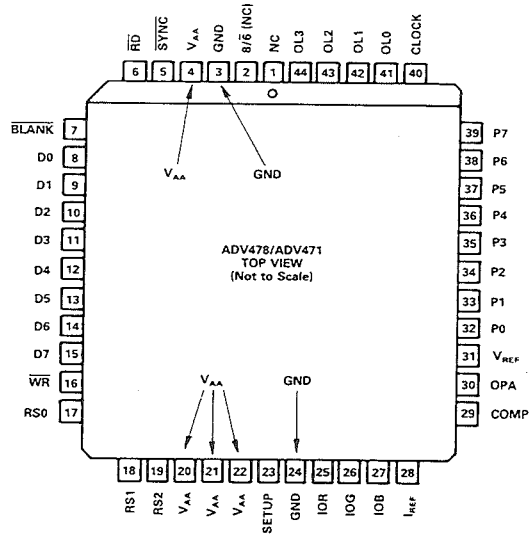
Many, if not all components required for a video graphics system are available as surface mount devices. Memories, controller chips and logic are all available in small SMT packages. Resistors and capacitors can also be purchased in a small "chip" format.

As well as producing Video RAM-DACs in a dual-in-line package (DIP), e.g., the ADV476 (28-pin DIP), Analog Devices packages its ADV478/ADV471 in 44-pin plastic leaded chip carriers (PLCC). This package has substantial advantages over DIP packages in that the lead-frame inductance is small (2-3 nH) and constant for any pin around the package. A DIP package usually has power and ground on diagonally opposing corner pins which presents a much larger lead-frame inductance (10–12 nH). Additionally lead-frame inductance varies with pin position.

In addition to the PLCC package the ADV478/ADV471 video DACs have a number of design features intended to minimize EMI problems.

The pinout of the ADV478/ADV471 in Figure 20 shows four power pins and two ground pins. In operation, the four V_{AA} pins are tied together at the package and supplied with a single +5 V supply. Similarly the two ground pins are tied together at the package and connected to the PCB ground. Internally, however, power rail routing has been separated according to functionality. The various V_{AA} pins are used to drive different internal sections of the ADV478/ADV471. One V_{AA} pin provides a common power rail for "digital" logic;

another provides an "analog" power rail for the DAC and reference circuitry; while yet another provides power to the n-substrate of the device. Since all p-channel transistors have as their back-gate the n-substrate, a separate substrate supply acts to isolate the DAC power rail from noise transients injected into the substrate by switching transistors. The use of multiple power and ground pins results in reduced voltage spiking and improved power supply rejection at the DAC outputs.

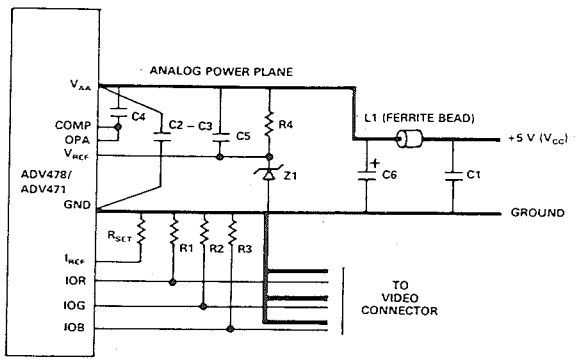


1. PIN NAMES FOR THE ADV471 INDICATED IN PARENTHESES
2. NC = NO CONNECT

Figure 20. ADV478/ADV471 PLCC Pin Assignment Showing Multiple Power and Ground Connection Points

CIRCUIT LAYOUT FOR THE ADV478/ADV471

A recommended layout and component listing for the ADV478/ADV471 is shown in Figure 21. More details regarding the characteristics of various decoupling and filtering components can be found in Appendix 1 of this application note.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1 μF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10 μF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75 Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R4	1 kΩ 5% RESISTOR	
R_{SET}	1% METAL FILM RESISTOR	
Z1	1.235 V VOLTAGE REFERENCE	ANALOG DEVICES AD589KH

Figure 21. Connection Diagram and Component Listing for the ADV478/ADV471

GETTING FCC CERTIFICATION

The final chapter in EMI design is the actual test. With good design practice and even a partial adherence to some of the issues raised in this application note, no difficulty should be encountered in achieving certification. The testing itself however must be carried out with great care in order to do justice to your design. It should be remembered that in the case of a peripheral device such as a VGA board, FCC testing is applied to a complete operating computer system. This complete system must pass with the VGA board present before the VGA board itself is considered to have passed.

A complete operating computer system is configured using the following:

1. a PC compatible computer with keyboard
2. a printer connected to the printer port
3. a mouse or modem connected to the serial port
4. a monitor.

The PC and all its peripherals must be operating when measurements are made.

It is paramount that only the best equipment is used. If for example a noisy monitor is used, the test results might not pass the agency limits, not because your board is at fault, but perhaps because of a poor quality, noisy monitor used in the test. An excellent choice of monitor is IBM's 851X series. Another principal culprit, causing EMI in such a system, is the parallel printer cable. A good quality, shielded cable must be used.

If you are using an outside test house, it is advisable to be present during testing, or at least have a representative from your company who understands the operation of the system and its various components.

AD/VGA

Analog Devices has designed its own high performance graphics board, AD/VGA for evaluation purposes. The board design is based on the ET3000AX* Video Graphics Controller from Tseng Labs and the high performance ADV478/ADV471 Color Palette RAM-DAC from Analog Devices. The board is fully compatible with all IBM PC† video standards as well as IBM PS/2† Video Graphics Array (VGA). It has additional modes including 800 × 600 resolution with 256 colors as well as 1024 × 768 in 16 colors. These modes require pixel data rates of up to 45 MHz or 66 MHz. The silkscreen showing component placement and type for the AD/VGA board is shown in the appendix.

The board has been certified to comply with the limits for a Class B computing device pursuant to Subpart J of Part 15 of FCC Rules.

FCC ID: HRF55L8826VGA

One actual set of measurements for radiated emissions from the AD/VGA board is shown in Appendix 2. Results can be compared to the FCC limits as listed in Table I.

The AD/VGA board was installed in a DELL SYS 200‡ computer using an IBM 8514 monitor. A modem, printer and mouse were attached. These measurements were made in 132 × 44 text mode.

A complete set of test results is available for inspection.

REFERENCES

1. International EMI Emission Regulations

USA:	FCC–15 Part J
West Germany:	VDE 0871/VDE 0875
Canada:	CSA C108.8–M1983
Japan:	CISPR(VCCI)/PUB 22

2. EMI Countermeasures – Application Guidance – Murata Mfg. Co. Ltd.
3. Henry. W. Ott, "Noise Reduction Techniques in Electronic Systems." John Wiley, N.Y., 1986.
4. Paul A. Brokaw, "An I.C. Amplifier Users' Guide to Decoupling, Grounding and Making Things Go Right for a Change." Analog Devices Data-Acquisition Databook 1984, Volume 1, Pages 20–13 to 20–20.
5. Motorola Inc., "MECL Design Handbook" 2nd Edition, 1972.

10

†IBM PC, IBM PS/2, IBM8514/A and VGA are trademarks of International Business Machines Corp.
‡DELL SYS 200 is a trademark of Dell Computer Corporation.
*ET3000AX is a trademark of Tseng Laboratories, Inc.

APPENDIX 1

EMI FILTERING COMPONENTS

No matter how well a PCB is laid out, there will always be a need for some kind of filtering. This section of the application note examines, in some detail, a number of filtering devices which are suitable for a high speed graphics system. The frequency characteristics of such devices as well as their inherent limitations will be discussed.

The effect of an EMI filter is generally expressed in terms of insertion loss. Noise suppression is described as a logarithm of the ratio of the output voltage without a filter to that with a filter in the circuit and is normally expressed in units of dBs. The simplest example is a first order device, a parallel capacitor or series inductor. A first order filter has an insertion loss slope of 20 dB per decade.

Table 1-1 shows a list of suitable filtering devices and their useful frequency bandwidth.

Filtering Device	Effective Bandwidth
Two-Terminal Capacitor	100 kHz–50 MHz
Ferrite-Bead Inductor	10 MHz–500 MHz
Three-Terminal Capacitor	1 MHz–800 MHz
Four-Terminal LC Filter	100 kHz–1 GHz

Table 1-1. Effective Bandwidth of Various Filtering Devices

The favorite and most widely used filtering device in electronic apparatus today is undoubtedly the "Bypass-Capacitor." It is simple to use, very effective and cheap. Unfortunately though, its effect in a high frequency graphics systems is sometimes the opposite to what is desired. A little thought regarding choice of capacitor, in terms of construction and value can lead to a dramatic improvement in noise performance.

Two-Terminal Capacitor

Let us first take a more detailed look at the structure of a real capacitor.

The impedance of an ideal capacitor connected between line (V_{CC}) and ground is given by

$$Z_C = \frac{1}{2\pi f C.}$$

From Figure 1-1, we can see that the insertion loss of an ideal capacitor increases with frequency at a rate equal to 20 dB/decade. In other words, the capacitor's filtering effect is greatest for higher value frequency components. Increasing the value of capacitance has the effect of filtering out lower frequency components. In the real world, however, a two-terminal capacitor has inductance in series with the capacitance, due to the inherent inductance of the lead wires as shown in Figure 1-2. The reactance characteristic of such a capacitor is shown in Figure 1-3 with the composite insertion loss characteristic shown in Figure 1-4. Clearly, the inductance, ESL, limits the insertion loss. The residual inductance of a capacitor is a function of both the electrode construction as well as lead length. This inductance can vary between 5 nH and 150 nH.

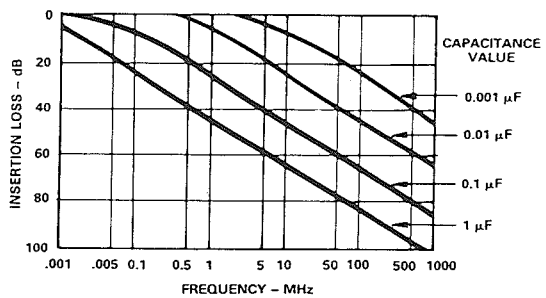


Figure 1-1. Insertion Loss Versus Frequency for Ideal Capacitors

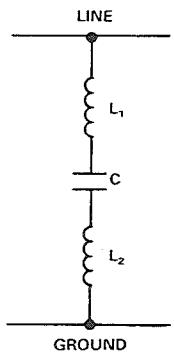


Figure 1-2. Real Capacitor Showing ESL Due to L_1 and L_2

Table 1-2 shows typical values of series inductance for various capacitor types.

Capacitor Type	Capacitance µF	Equivalent Series Inductance (ESL) nH
Lead Type Monolithic Ceramic	0.01	5
	0.1	5
	1.0	6
Disc/Lead Type Ceramic	0.0002	4.5
PolyethyleneTelephthalate	0.03	9
Mica	0.01	52
Polystyrene Film	0.001	12
	0.1	100
Tantalum Electrolytic (with Solid Electrolyte)	16	5
Aluminum Electrolytic		
RF Specific	470	13
Standard	470	130

Table 1-2. ESL for Various Capacitor Constructions and Values

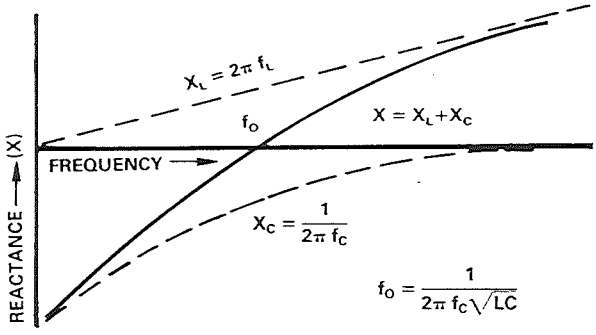


Figure 1-3. Reactance Characteristic of a Capacitor with Finite ESL

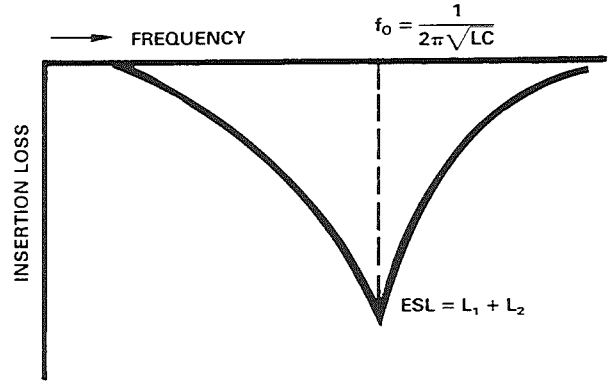


Figure 1-4. Insertion Loss of a Capacitor is Limited by f_O

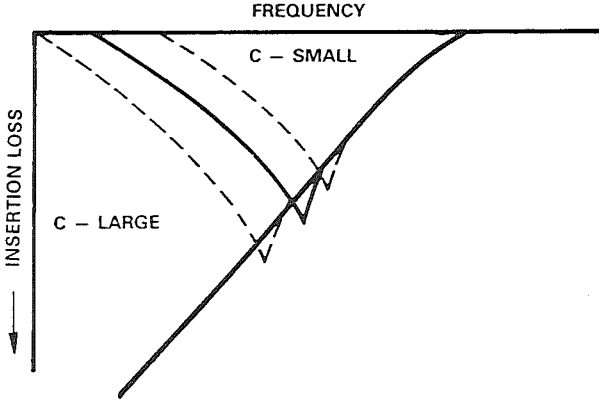


Figure 1-5. A Large Value Capacitor Has a Decreased f_O

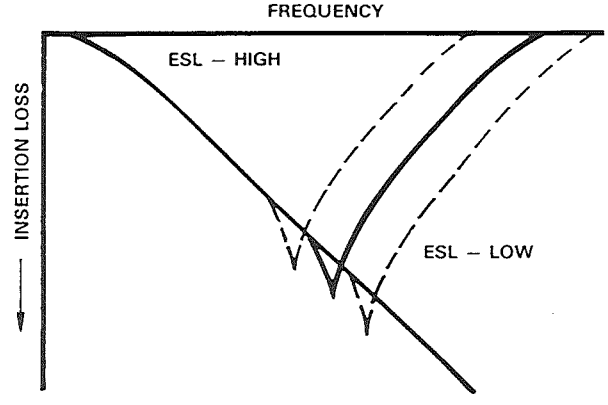


Figure 1-6. A Capacitor with Low ESL Has an Increased f_O

The resulting effect of this equivalent series inductance (ESL) is a reduction in the effectiveness of the capacitor at filtering frequency components beyond a certain point, known as the resonant frequency, f_O. It can be seen from Figures 1-4 to 1-6 that increasing the capacitance value can have the effect of reducing the resonant frequency thereby reducing the ability of this device to filter out higher frequency components. It is therefore imperative that a capacitor with low residual inductance be used. A good choice of high frequency decoupling capacitor would be a 0.1 μF lead type monolithic ceramic capacitor (MCC). This has a series inductance of approximately 5 nH. The resonant frequency, f_O, is thus kept high thereby maximizing high frequency rejection.

As well as series inductance, a capacitor will also contain resistance, referred to as equivalent series resistance (ESR). See Figure 1-7.

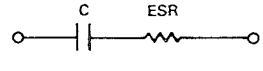


Figure 1-7. Real Capacitor showing ESR

This resistance imposes a finite limit on the ability of a capacitor to bypass high frequencies to ground. Total impedance of the device can never be lower than that imposed by the equivalent series resistance. A capacitor having a high ESR will exhibit a flattened insertion loss curve, compared with the sharp resonant point typically observed in capacitors with lower ESR values.

The overall equivalent circuit of a two-terminal capacitor with ESL and ESR is shown in Figure 1-8.

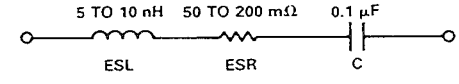


Figure 1-8. Equivalent Circuit of a Real Capacitor

Maximum noise reduction will be achieved through the selection of capacitors with lowest ESL and ESR values.

At least one decoupling capacitor should be used for each IC in the system. In the case of the Video RAM-DAC, it is recommended that for high frequency suppression, a 0.1 μF ceramic capacitor be used to decouple

each group of V_{AA} pins to ground. Low frequency components can be decoupled through the use of a 10 μF tantalum capacitor. Figure 21 shows the recommended decoupling scheme for the ADV478/ADV471. Capacitors with minimal lead length, should be placed as close as is physically possible to the device.

Three-Terminal Capacitor

Three-terminal capacitors have filtering characteristics extending to several hundred MHz. Two leads at the line side of the capacitor provide line input and output respectively, see Figure 1-9. This reduces effective series inductance.

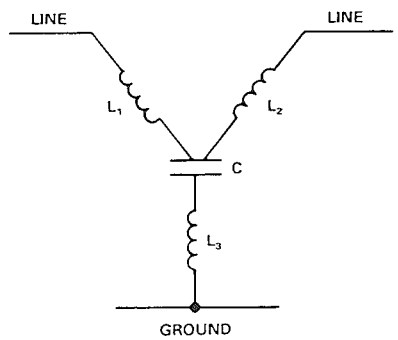


Figure 1-9. Equivalent Circuit of a Three-Terminal Capacitor

One particular example of the use of such a three-terminal device would be at the analog outputs of the Video RAM-DAC. The NFV510 series of three-terminal capacitors from Murata have a sharp insertion loss characteristic. This means that high frequency signals can be filtered without affecting the integrity of the signal itself. The NFV510 series has an excellent shape factor, due to an inherent roll-off of 100 dB/decade, see Figure 1-10. It therefore suppresses noise without reducing resolution. In the case of a graphics system with video output rates of 80 MHz, the NFV510-655 T2A 107 could be employed at the outputs of each of the red, green and blue DACs.

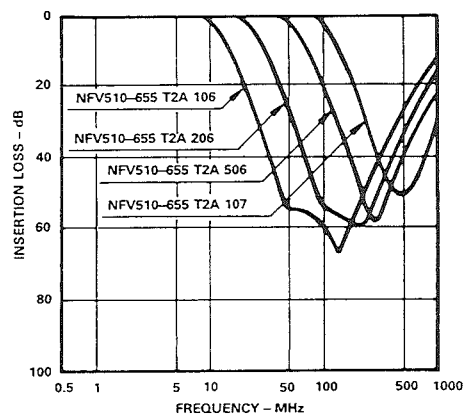


Figure 1-10. Frequency Response of the NVF510 Series of Three-Terminal Capacitors

Ferrite Bead Inductor

A ferrite is another very useful component in the effective suppression of EMI. One can consider a ferrite bead as a high frequency resistor with no resistance at dc. Ferrites have filtering characteristics which extend well into the megahertz range. They can be used to provide isolated power planes, e.g., a PCB's power plane may be subdivided into an analog power plane (V_{AA}) and clock circuitry power plane, see Figure 18. Ferrite beads work both ways; one prevents noise components on the PCB power plane from being coupled onto the analog power plane, while the other filters out noise components from the clock circuitry. The analog power plane provides power to the Video RAM-DAC and all its associated analog circuit, while the clock circuitry power plane provides power to the crystal oscillators and clock divide circuitry.

It is not, however, recommended to use a ferrite bead in separating ground planes; a separate analog ground plane to the Video RAM-DAC may have disastrous effects on the contents of the on-board color look-up table. One common ground plane should encompass the entire PCB.

The system's shield ground or earth may be connected through a ferrite bead to the regular PCB ground.

Ferrite is the generic term given to a class of non-conductive ceramics. They are constructed using combinations including oxides of iron, cobalt, nickel, zinc, magnesium and some rare earth materials. It is important to be careful in choosing ferrite beads. Ferrite composition and therefore filtering characteristics can vary quite significantly from manufacturer to manufacturer. Analog Devices recommends the use of the BL01/02/03 series of ferrite bead inductors from Murata as well as the Fair-Rite 2743001111. The frequency characteristic of a radial single bead ferrite bead is shown in Figure 1-11.

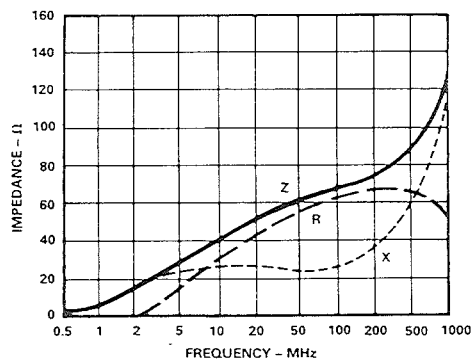


Figure 1-11. Frequency Characteristic of the BL01RN Ferrite Bead Inductor

DC Power Filter

In some cases it might be necessary to filter the power source's high frequency components. This is often the case when switched mode power supplies are used. If it is found that the system's power supply is excessively noisy, one could consider the use of a dc power filter

such as a BNX002-01 from Murata or equivalent. This filter which consists of a large value monolithic 4-terminal capacitor, a feed-through capacitor and beads, as shown in Figure 1-12, produces an effective filtering effect, 40 dB min over the frequency range 1 MHz to 1 GHz. Figure 1-13 shows the filtering characteristic of the BNX series of power filters from Murata.

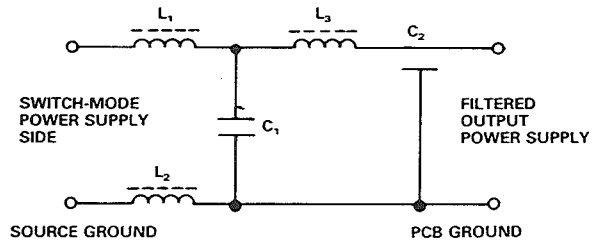


Figure 1-12. Equivalent Circuit of a dc Power Filter

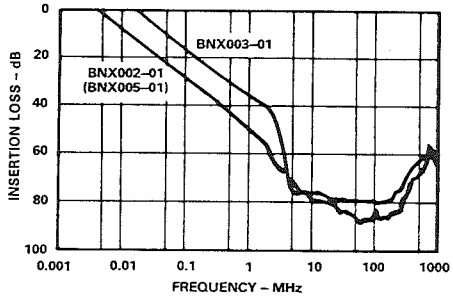


Figure 1-13. Frequency Response of the BNX Series of dc Power Filters

APPENDIX 2

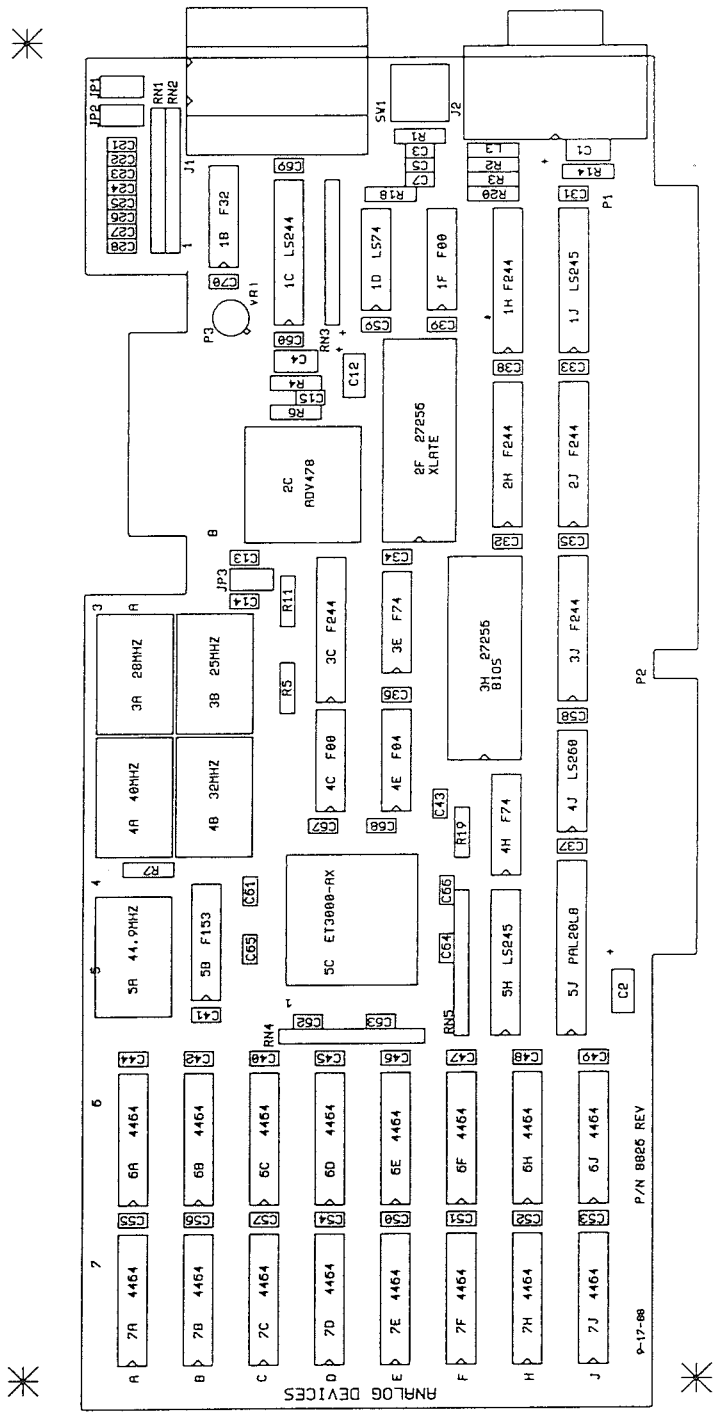
FCC TEST RESULTS OF AD/VGA

Frequency	EUT Orientation	Ambient Radiation	Antenna		EUT Radiation			Field Strength
			Polarization	Height	Factor	Maximum	Corrected	
MHz	Degrees	dB μV	H/V	Meters	dB/M	dB μV	dB μV/M	μV/m
37.2	60	6.7	V	1	12.9	18.8	31.7	38.5
48.1	20	3.6	V	1	12.9	19.0	31.9	39.5
60.6	90	7.8	V	1	11.4	20.3	31.7	38.5
62.8	90	9.8	V	1	10.6	17.3	27.9	24.8
69.5	50	8.6	V	1	8.9	19.9	28.8	27.5
70.9	30	10.8	V	1.5	8.9	24.0	32.9	44.2
72.7	90	10.9	V	1	8.6	20.1	28.7	27.2
75.8	30	14.2	V	1	8.4	22.4	30.8	34.7
78.9	30	13.1	V	1	8.4	24.5	32.9	44.2
80.7	0	10.9	V	1	8.5	19.1	27.6	24.0
88.0	0	12.0	V	1.5	10.0	22.1	32.1	40.3
119.7	330	4.4	H	1.5	15.8	16.9	32.7	43.2

Sample of FCC Test Results for AD/VGA Board

APPENDIX 3

AD/VGA COMPONENT PLACEMENT (SILKSCREEN)



ANALOG DEVICES

APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

Animation Using the Pixel Read Mask Register of the ADV47X Series of Video RAM-DACs

by Bill Slattery & Eamonn Gormley

INTRODUCTION

The Pixel Read Mask Register, which is an integral part of IBM's VGA* graphics system, can be used as a hardware-level Pixel Processing Unit. This allows real time motion or animation to be implemented with minimal software overhead. This application note examines the operation and structure of such a pixel processing unit with the pixel read mask register as the central controller. A practical application which uses the pixel read mask register to animate a picture scene is described. A complete listing of the Turbo-C source code is given in the appendix.

No additional hardware is required for existing VGA graphics systems to implement this application.

VIDEO RAM-DAC

Analog Devices produces a range of video RAM-DACs, which are specifically designed for IBM's Personal System/2* VGA. The range includes the ADV478, ADV471 and ADV476, all of which are monolithic +5 V CMOS video RAM-DACs. These parts are specified over a number of speed grades; 35 MHz, 50 MHz, 66 MHz and 80 MHz. The RAM-DACs are packaged as 44-pin PLCC and 28-pin plastic DIP devices.

The ADV471 and ADV476 each contain a triple 6-bit digital-to-analog converter and a 256 location by 18 bits deep color look-up table. The devices also include an asynchronous pixel input port and bidirectional microprocessor (MPU) port. These devices and the associated control circuitry allow for flexible interface to many graphics systems configurations. The ADV478 differs from the ADV471 only in terms of its color resolution. The ADV478 has a triple 6-bit/8-bit D/A converter with a 256 × 24/18 color look-up table. The color resolution of the ADV478 is user selectable between 6 bits and 8 bits. The higher 8-bit performance can be used with IBM's 8514/A* graphics standard (upgrade on standard VGA). More detailed information on these and other video RAM-DACs can be obtained in the relevant product data sheets.

Built into all three devices is an 8-bit register known as the Pixel Read Mask Register. Figures 1 and 2 are block diagrams of the ADV478/ADV471 and ADV476 which show the Pixel Read Mask Register.

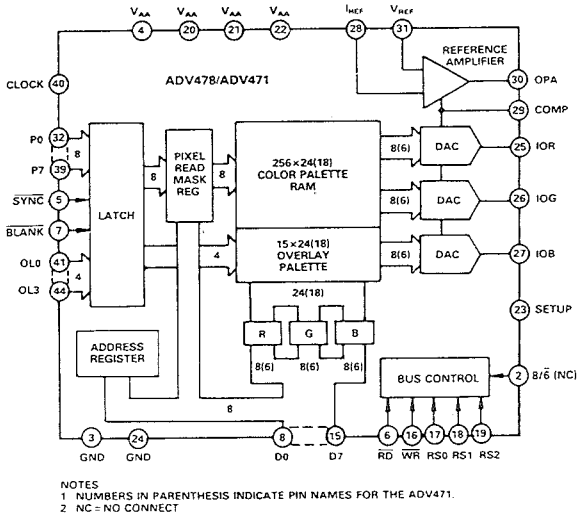


Figure 1. ADV478/ADV471 Functional Block Diagram

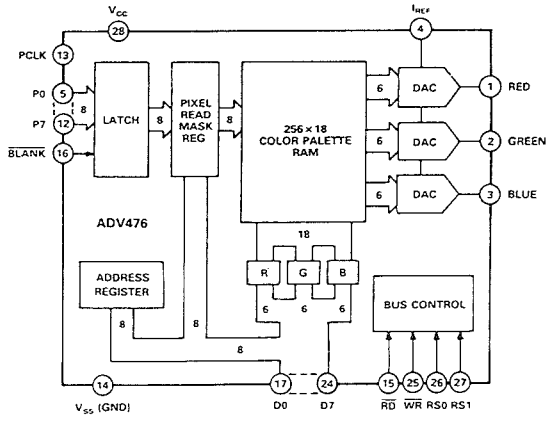


Figure 2. ADV476 Functional Block Diagram

*IBM, VGA, Personal System/2 and 8514/A are trademarks of International Business Machines Corp.

10

Some of the uses to which the Pixel Read Mask Register can be put include on-screen special effects such as real time animation, flashing objects and overlays.

PIXEL READ MASK REGISTER

The Pixel Read Mask Register is placed in the path of the pixel input stream of data as shown in Figure 3.

The input pixel data stream (P0–P7) is gated with the contents of the Pixel Read Mask Register. The operation is a bitwise logical ANDing of the pixel data. The contents of the Pixel Read Mask Register can be accessed and altered at any time by the MPU (D0–D7). Table I shows the relevant control signals. Under normal operating conditions, this register is loaded with all 1s, i.e., transparent mode.

In a VGA graphics system, the Pixel Read Mask Register is memory mapped and is accessible (read/write) by addressing memory location 36CH.

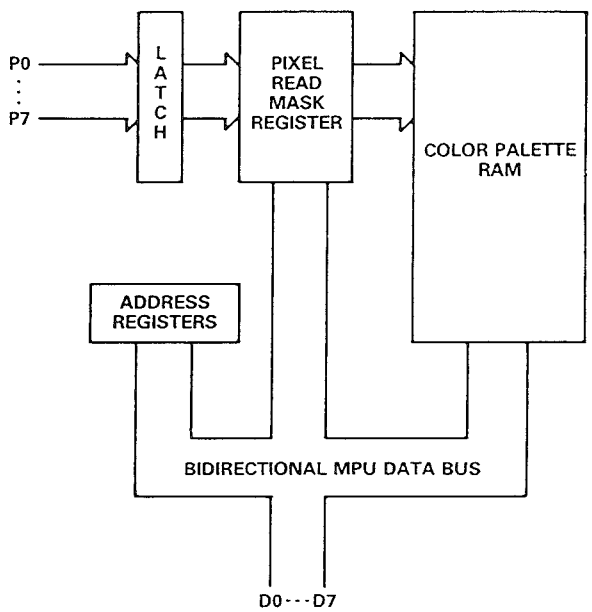


Figure 3. Video RAM-DAC Pixel & Data Ports Showing the Pixel Read Mask Register

RS2*	RS1	RS0	Addressed by MPU
0	0	0	Address Register (RAM Write Mode)
0	1	1	Address Register (RAM Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register

*RS2 is only present on ADV478/ADV471

Table I. Control Input Truth Table for Video RAM-DAC

Figure 4 shows the internal architecture of the pixel input port. The input word Pi, which corresponds to an on-screen pixel location, is ANDed with the contents of the Pixel Read Mask Register, Pm.

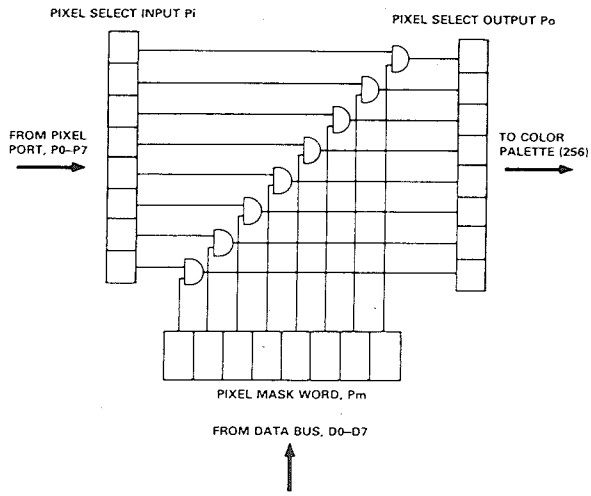


Figure 4. Internal Architecture of Pixel Input Port

The resulting output word, Po, determines which location in the color palette will be assigned to a particular on-screen pixel. Figure 5 shows the logical diagram for this masking operation.

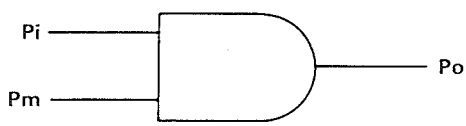


Figure 5. Equivalent Logical Representation of Masking Operation

$$Po = Pi \cdot Pm \quad (1)$$

If Pm = 1, transparent mode, then

$$Po = Pi \quad (2)$$

The pixel stream of data, Po, which arrives at the color palette is a function of both the pixel input stream, Pi, from the Frame Buffer and the contents of the Pixel Read Mask Register, Pm. In the case of an animation application, which will be discussed later in this application note, the rate at which the pixel mask word is changed will determine the motion speed of the scene.

This pixel masking operation can be used to alter the displayed colors without changing the contents of either the video Frame Buffer or the Color Palette RAM. One interpretation of this operation is to consider the pixel input structure of the video RAM-DAC as an on board Pixel Processing Unit.

PIXEL PROCESSING UNIT

The Pixel Input Port (Pi), Pixel Read Mask Register (Pm) and Data Input Port (MPU) within the video RAM-DAC, are the hardware components of this Pixel Processing Unit (PPU). An associated software routine to control the operation is the final element in the complete PPU system. This interpretation enables the color palette to be configured as a multidimensional, paged memory address space, see Figure 6.

In the case of the ADV471 and ADV476 the color palette can be perceived as being broken into an even number of 18-bit color planes instead of just one 18-bit deep color plane. (In the case of the ADV478, each plane is 24 bits deep.)

The palette can therefore be partitioned to produce up to a total of 256 discrete contiguous color memory planes, some of which are shown in Figure 6. A tradeoff, however, must be considered when dividing the color palette into multiple color planes. The number of simultaneously displayable screen colors is inversely proportional to the number of color planes within the color palette. Table II illustrates this relationship. This contiguous configuration is not, however, the sole way of segmenting the memory within the palette. Other non-contiguous configurations including interleaving can be implemented. The choice of memory configuration will be determined by the particular application so as to make most efficient use of the available video memory (Image Frame Buffer and Color Palette RAM).

Number of Color Planes	Number of Simultaneously Displayable Colors
1	256
2	128
4	64
.	.
.	.
256	1

Table II. Simultaneously Displayable Screen Colors versus Number of Color Planes

To operate the PPU, two principal steps must be taken:

1. Load the image data in the correct paged configuration to both the frame buffer and color look-up table, e.g., four frame composite images to the frame buffer corresponding to four discrete planes of color to the palette RAM.
2. Generate the corresponding pixel mask words. These words are individually written to the Pixel Read Mask Register, Pm (at VGA memory location 36CH) and select which of the color planes is to be assigned to the incoming pixel data stream. In the case where four planes are implemented (see Figure 6), four pixel mask words are required.

The overall VGA System Block Diagram showing the PPU and an associated 8-page memory configuration of the color palette is shown in Figure 7.

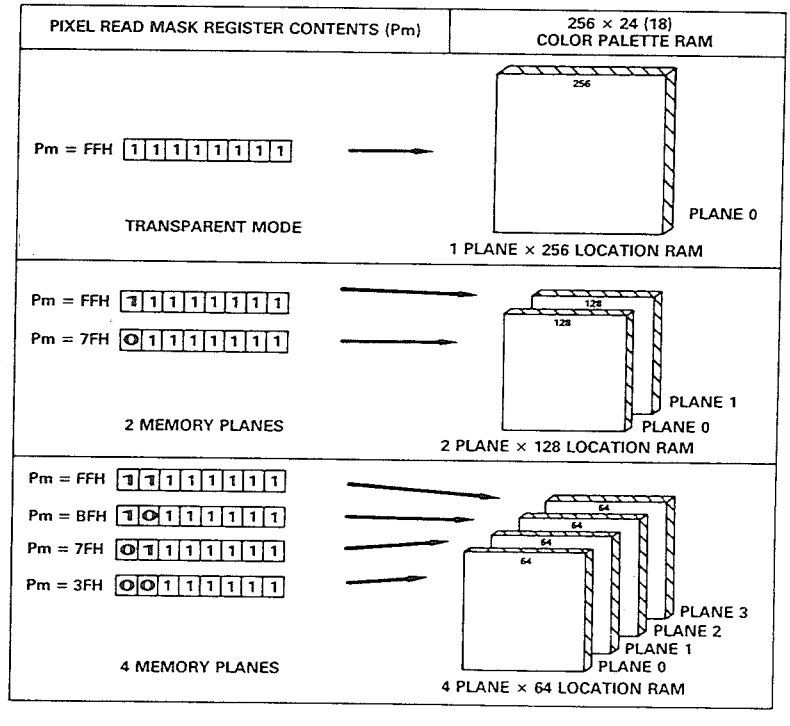


Figure 6. Some Color Palette RAM Configurations Showing Paged Memory Planes and Associated Pixel Read Mask Word (Pm)

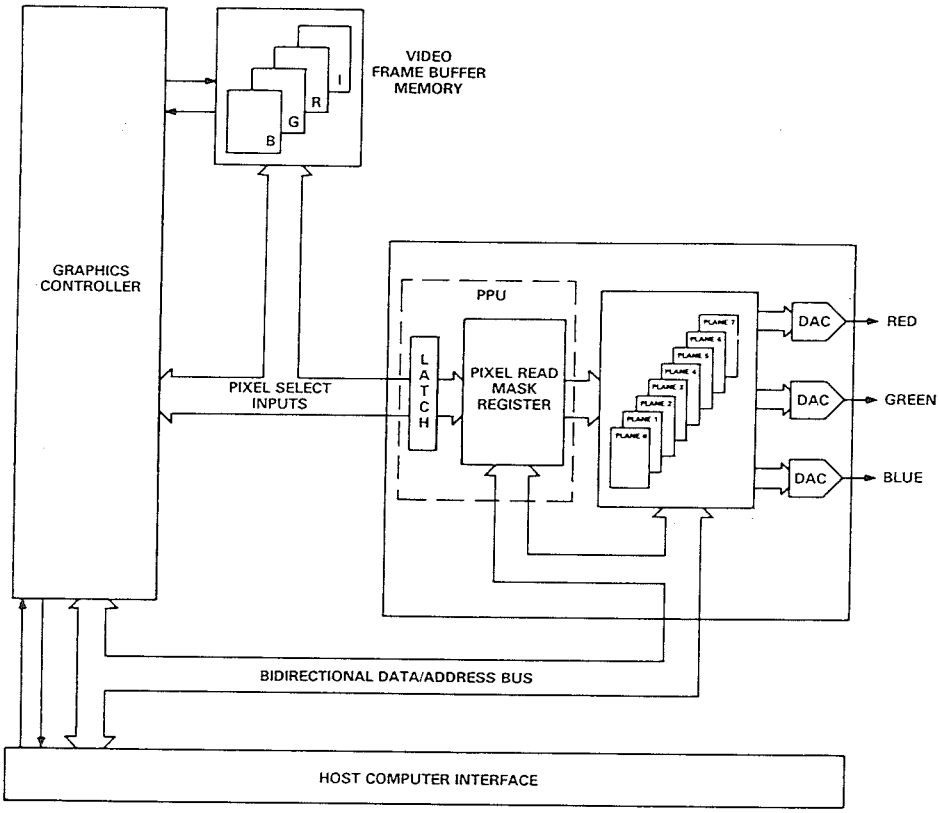
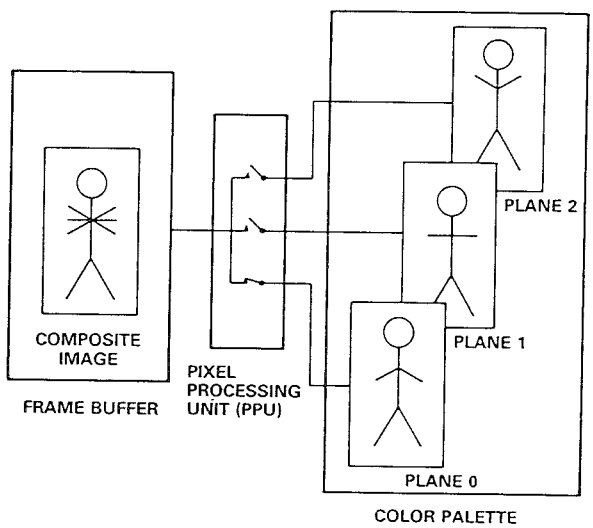


Figure 7. VGA System Block Diagram Showing Color Palette Broken into a Number of Color Planes

ANIMATION

Real time animation using the Pixel Processing Unit is based on the principle that rapidly changing the colors of a stationary object gives the illusion of motion. In other words, a number of similar images or frames, differing only by the relative position of the various colors, displayed in quick succession, can result in motion.

A simple example to explain the idea of animation is illustrated opposite. The animated image consists of three frames; each of the three frames is initially drawn as one composite picture (Frame Buffer image). The color palette contains three discrete, memory blocks or planes of color information, corresponding to three stages of animation. The animation effect in this example is "arm waving" of the cartoon character. By assigning the color planes one by one to the image in the Frame Buffer, the effect of animation can be perceived on the screen. The color plane assigned to the composite image is determined by the PPU which is controlled by the word in the Pixel Read Mask Register. Frame 1 is assigned Color Plane 0, this colors the down arm position in black, while the up and horizontal arm positions take on the background color. Frame number 2 is assigned Color Plane 1, this colors the horizontal arm position in black while the other two arm positions are assigned the back ground color.



Finally, Frame 3 takes on Color Plane 2. This process is then repeated giving the illusion of motion. The rate at which each frame is selected determines the rapidity of the arm waving.

ANIMATION USING THE PPU

This section describes a particular animation example. The scene used in this example consists of traveling space ships and rotating planets. The program which draws the scene and implements the animation is described in the flow diagram of Figure 8. The associated source code, written in Borland's Turbo-C, is given in the Appendix. This application implements 8-stage animation.

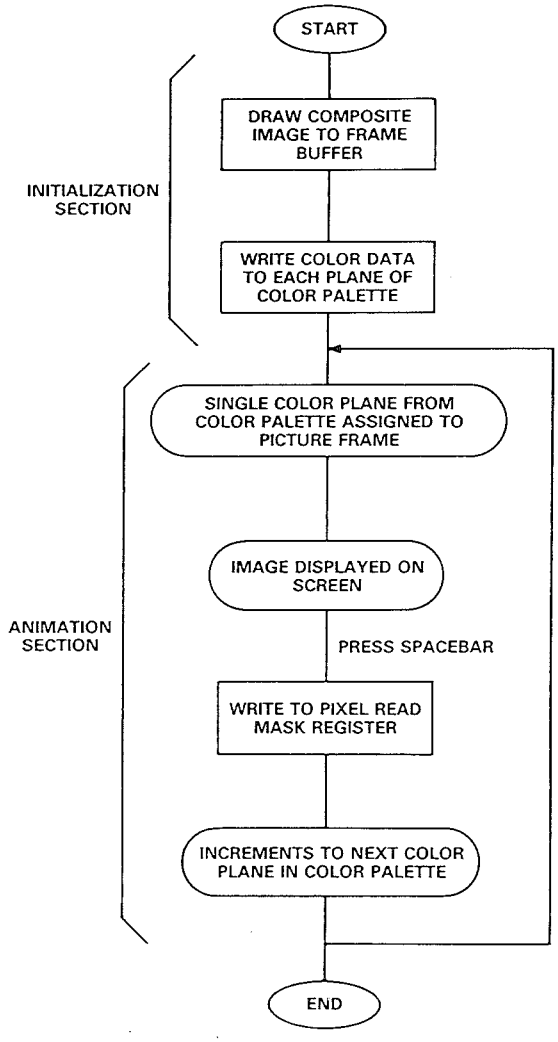


Figure 8. Flow Diagram Representation of Animation Using the PPU

The complete image is drawn to the Frame Buffer. This composite picture contains eight frames of information. The corresponding color planes for each of the eight frames in this composite image, are drawn to the color palette. The color information is arranged in a paged memory format corresponding to that shown in Figure 7. Each of these eight color planes has similar color data; they differ from each other only in terms of the relevant position of the particular colors. For example, Plane 0 could have blue in its first location and color yellow in its second location, while Plane 1 could have the opposite, yellow in Location 1 and blue in Location 2. During the display period, the color palette will only allocate colors to one of the eight frames (i.e., one color plane) at a particular instant. Each plane of color information is mapped to a particular frame within the Frame Buffer. The user-defined value of the Pixel Read Mask Register determines which of the color planes within the palette will be chosen for display at any particular instant. The hex codes, written to the Pixel Read Mask Register Pm, which correspond to each of the color planes (Plane 0 to Plane 7) are listed in Table III.

3C6F	: Address of Pixel Read Mask Register (Pm)	
8FH → Pm	: Plane 0 Selected	Pm = 1000 1111
9FH → Pm	: Plane 1 Selected	Pm = 1001 1111
AFH → Pm	: Plane 2 Selected	Pm = 1010 1111
BFH → Pm	: Plane 3 Selected	Pm = 1011 1111
CFH → Pm	: Plane 4 Selected	Pm = 1100 1111
DFH → Pm	: Plane 5 Selected	Pm = 1101 1111
EFH → Pm	: Plane 6 Selected	Pm = 1110 1111
FFH → Pm	: Plane 7 Selected	Pm = 1111 1111

Table III. Value Written to Pixel Read Mask Register and Associated Color Plane

Pressing the "Spacebar" increments the pixel read mask register corresponding to a jump of 16 locations in the color palette. As there are 16 colors in each color plane, a jump of 16 locations will select the corresponding color in the next highest plane. Continuously pressing the "Spacebar" cycles the incoming pixel stream of data through each of the eight color planes within the palette. This results in the apparent motion or animation of the image.

APPENDIX

C Program for ANIMATION EXAMPLE

Pixel Processing Using Video RAM-DACs
"Rotating Planets & Spaceships"

```
#include <stdlib.h>  /* Turbo C include files */
#include <math.h>    /* these are available under most versions */
#include <dos.h>     /* of C for the IBM & compatibles */
#include <graphics.h>
void palette(int col,int red,int green,int blue);
void plot13(int x,int y,int col);                /* function definitions */
void model3();
void circle13(int x,int y,int r,double tilt);
void planets();
void stars();
void line13(int x1,int y1,int x2,int y2,int col);
void triangle();

main()
{
 int gd=0,gm=0,opt;
 union REGS reg;
 detectgraph(&gd,&gm);                  /* check for a VGA card */
 if (gd != 9){
  printf("This program cannot find a VGA card installed in this computer.\n");
  printf("A VGA card is necessary to run the tests.");
  exit(1); }

 planets();                             /* do demo */
 reg.h.ah = 0x00;
 reg.h.al = 0x03;
 int86(0x10,&reg,&reg);                 /* return to text mode when finished */
}

void mode13()                           /* set up mode hex 13 = decimal 19 */
{                                       /* this is a 256 color mode with */
 union REGS reg;                        /* 320 x 200 pixel resolution */
 reg.x.ax = 0x0013;
 int86(0x10,&reg,&reg);                 /* set mode 0x13 */
}

void palette(int col,int red,int green,int blue)
             /* assigns a physical color to a logical color */
{
  union REGS reg;
     reg.x.ax = 0x1010;
     reg.x.bx = col;
     reg.h.dh = red;
     reg.h.ch = green;
     reg.h.cl = blue;
     int86(0x10,&reg,&reg);         /* call bios routine to change palette */
}

void plot13(int x,int y,int col)    /* special plot routine for mode 0x13 */
{
     union REGS reg;
     if(x>=0 && y>=0 && x <320 && y<200){
        reg.x.dx = y;               /* set up registers */
        reg.x.cx = x;
        reg.h.ah = 0x0c;
        reg.h.al = col;
        int86(0x10,&reg,&reg);      /* call bios plot routine */
     }}

void circle13(int x,int y,int r,double tilt)
{                                    /* routine draws a single planet */
```

```
int la,yy;
double ang,oldx,oldy,newx,newy,sintl,costl,rcos,rsin;
for(la = -r; la < r; la++)
{                                       /* routine uses a fairly simple */
 yy = sqrt(r*r - la*la) + 1;            /* algorithm to draw a solid circle */
 line13(la+x,y-yy,la+x,y+yy,14); }

costl = cos(tilt);                      /* set up some variables */
sintl = sin(tilt);
yy = 240;                               /* To draw lines of longitude: */
for(la = r; la >= -r; la-=r/15)         /* draw portions of ellipses */
  {                                     /* and rotate them by tilt radians */
   oldx = x-r*sintl;
   oldy = y+r*costl;
   for(ang = -1.57;ang <1.57;ang+=.195) {
    newx = x+la*cos(ang)*costl+r*sin(ang)*sintl;
    newy = y-r*sin(ang)*costl+la*cos(ang)*sintl;
    line13(newx,newy,oldx,oldy,yy); /* line segment of ellipse */
    oldx = newx;                        /* store endpoints */
    oldy = newy;  }
   yy = (yy==247) ? 240 : ++yy;         /* incrememt color used */
  }
for(ang=-1.57;ang<1.57;ang+=.39)        /* draw lines of latitude */
   {                                    /* ie sloped lines */
    rcos = r*cos(ang);
    rsin = r*sin(ang);
    line13(x+rcos*costl-rsin*sintl,y+rsin*costl+rcos*sintl
          ,x-rcos*costl-rsin*sintl,y+rsin*costl-rcos*sintl,15);
   }}

void planets()              /* routine to draw and animate the planets */
{
 int la,lb;

 model3();
 palette(7,255,255,255);
 printf("       Pixel Read Mask Demo\n");
 printf("     ==========================\n");
 printf("  This program contains an animated     picture scene which ");
 printf("is initially drawn  on the screen and then ANIMATED ");
 printf("using   the Pixel Read Mask Register.\n");
 printf("\n  Press the spacebar to draw scene and  hold it down ");
 printf("when scene is ready for    animation. When finished, ");
 printf("press any     other key.....");
 while(getch() != ' ');                 /* wait for keypress */

 model3();
 for (la=8;la<16;la++)                  /* set up the palette for animation */
   {
    for (lb=0;lb<8;lb++)
    palette(la*16+lb,0,10,63);          /* set planet lines to blue */
    for (lb=8;lb<16;lb++)
    palette(la*16+lb,0,0,0);            /* stars are initially black */
   }
 for (la=128;la<256;la+=17)
    palette(la,63,63,63),               /* define one line on planet to white */
    palette(la+8,63,63,0);              /* and one star to yellow, per frame */

 palette(15,255,255,255);               /* set color 15 to pure white */
 palette(7,20,255,0);                   /* color 7 to green */
 palette(14,0,10,63);                   /* color 14 used for planet background */

 stars();                               /* draw stars in background */
 circle13(30,30,30,0.9);                /* draw the actual planets */
 circle13(280,35,35,4.0);
 circle13(130,100,70,-0.8);
```

```
   circle13(40,240,125,0.5);
   triangle();                          /* draw the spaceship thingy */
   gotoxy(30,21);printf("Space to");
   gotoxy(30,22);printf("animate.");    /* on screen instructions */
   gotoxy(30,24);printf("Other key");
   gotoxy(30,25);printf("to stop.");
    la=143;                             /* 143 = %10001111 */
    do
     outportb(0x3c6,la),                /* this part does the actual animation */
     la = (la<255) ? la+16 : 143;       /* loop through the palette */
   while((lb = getch()) == ' ');        /* while the spacebar is being pressed */
}

void stars()                            /* routine to plot in the stars */
{
 int la,lb,lc,ld,le,col = 248;
 long q;
 srand(time(&q) % 37);                  /* set up random background */
 for (la=0;la<200;la+=5)  {
    lc = (rand()&0x7)-0x4;
    ld = la;
    le = (rand()&7)+3;
    for (lb=1;lb<320;lb+=le,ld=la+lc*lb/64)
       plot13(lb,ld,col),     /* plot the star */
       col = (col == 255) ? 248 : ++col;
  }}

void line13(int x1,int y1,int x2,int y2,int col)
{                                       /* this routine draws a line in */
 int la,lb,lc;                          /* graphics mode 13H */
 if (abs(x1-x2) > abs(y1-y2))  {       /* line longer in x or y direction ? */
   lc = (x2-x1);lb = (x2 - x1 >=0) ? 1 : -1;
   for (la=x1;la!=x2;la+=lb)            /* loop works out the points on */
   plot13(la,y1+(la-x1)*(y2-y1)/lc,col);   /* the line and plots them */
  }
  else  {
   lc = (y2-y1);lb = (y2 - y1 >=0) ? 1 : -1;
   for (la=y1;la!=y2;la+=lb)
   plot13(x1+(la-y1)*(x2-x1)/lc,la,col);
  }}

void triangle()          /* This routine draws a simple spacecraft-type */
{                        /* object for animation. */
 int la,lb=19,col=248;   /* starting size = 19, color = 248 */
 double tilt=0.5236;     /* starting tilt */

 for (la=200;lb>0;la-=lb,lb--,tilt += .3)
 {                       /* loop to draw 19 objects */
  line13(200+la/2+lb*cos(tilt),la+lb*sin(tilt),
         200+la/2+lb*cos(tilt+2.0944),la+lb*sin(tilt+2.0944),col);
  line13(200+la/2+lb*cos(tilt+2.0944),la+lb*sin(tilt+2.0944),
         200+la/2+lb*cos(tilt+4.1888),la+lb*sin(tilt+4.1888),col);
  line13(200+la/2+lb*cos(tilt+4.1888),la+lb*sin(tilt+4.1888),200+la/2,la,col);
  line13(200+la/2,la,200+la/2+lb*cos(tilt),la+lb*sin(tilt),col);
  col = (col==255) ? 248 : ++col;    /* col = col + 1 until col = 255, when */
 }}                                  /* col returns to zero */
```