Signal Path	tpd	Max Trace Len	
Reset Q Counter	7.5	12.0"	
FetchMicrocode	8.5	6.0"	
DECODE (uCODE)	9.0	3.0"	
DECODE (OP)	8.8	4.5"	
ResetIR	8.2	7.8"	
ALU (ADDRESS)	9.2	1.8"	Critical routing required
ALU (DATA)	7.7	10.8"	
ALU (BCD1)	7.5	12.0"	
ALU (BCD2)	6.9	15.6"	
Carry Recirculate	8.3	7.2"	
Evaluate Flags (Implied)	8.8	4.2"	
DECODE (uCODE) FLG.MX	6.7	16.8"	
BranchTest (Implied)	8.9	3.6"	
Exit Carry Clear (EXIT.CC)	9.3	1.2"	Critical routing required
Repeat Carry Set	6.5	18.3"	
Incrementer 16-Bit	8.0	9.3"	
Synch Read	8.3	7.5"	
Asynch Read (Wait-State)	6.9	15.5"	
Asynch Write (Wait-State)	5.9	21.6"	

Critical Routing		3.0 Inches
Max Cycle		10.0 ns
Clock-Skew		0.5 ns
Critical Path	Register Logic = AVC	9.3 ns
Max Frequency Estimate (MHz)		**107.5 MHz**

Note: tpd figures shown are "Typical" when those are available, or calculated as the mid-point between MIN and MAX otherwise.

Note: LVC, ALVC and CBTLV propagation times at (50pf, 25˚C, 3.3V) unless otherwise noted.

Note: AVC propagation times at (30pf, 25˚C, 3.3V) unless otherwise noted.

Note: AUC propagation times at (15pf, 25˚C, 2.5V) unless otherwise noted.

Component Inventory

	Component	Description	TPD		Datasheet
	74AUC00	NAND - tpd	0.8	ns	
	74AUC02	NOR - tpd	0.9	ns	
	74AUC04	NOT - tpd	0.3	ns	
	74AUC08	AND - tdp	0.9	ns	
	74AUC16374 E	Register - Enable	1.5	ns	
	74AUC16374 S	Register - Setup	0.6	ns	2.1
	74AUC16374 T	Register - CLK to Q	1.5	ns	
	74AUC1G86	XOR - tdp	0.8	ns	
TI	74AUC2G53 E	Fet Switch - Select	1.6	ns	
TI	74AUC2G53 S	Fet Switch - Select	1.1	ns	
TI	74AUC2G53 T	Fet Switch - Data to Y	0.1	ns	
	74AUC32	OR - tdp	0.8	ns	
	74AUC32	OR - tdp	0.9	ns	
	74AUC74 S	Flip-Flop – Setup	0.7	ns	
	74AUC74 T	Flip-Flop – Clk to Q	1.0	ns	
	74AUC86 T	XOR - tpd	0.8	ns	
Mouser – NXP	74AVC16374 E	Register - Enable	2.0	ns	
Mouser – NXP	74AVC16374 S	Register - Setup	0.0	ns	
Mouser – NXP	74AVC16374 T	Register - CLK to Q	1.3	ns	
NXP	74CBTLV3245 E	Buffer - Enable	3.4	ns	
NXP	74CBTLV3245 T	Buffer - tpd	0.25	ns	
IDT	74CBTLV3251 D	MUX - Data to Y	0.25	n	
IDT	74CBTLV3251 E	MUX - Sel to Y	3.5	ns	
IDT	74CBTLV3251 S	MUX - Sel to Y	2.8	ns	
NXP	74CBTLV3253 D	MUX - Data to Y	0.25	ns	
NXP	74CBTLV3253 S	MUX - Sel to Y	2.0	ns	
NXP	74CBTLV3257 D	MUX - Data to Y	0.25	ns	
NXP	74CBTLV3257 S	MUX - Sel to Y	3.2	ns	
NXP	74LVC138 E	Decoder - Enable	2.9	ns	
NXP	74LVC138 S	Decoder - A to Y	2.7	ns	
NXP	74LVC161 R	Counter - Reset	3.2	ns	
NXP	74LVC161 S	Counter - Setup	2.5	ns	
NXP	74LVC161 SL	Counter - Load	3.0	ns	
NXP	74LVC161 T	Counter - CP to Q	3.6	ns	
Atmel	ATF16V8 T	PLD - I to O	5.0	ns	
TI	CDCVF310 S	Clock Buffer Skew	0.5	ns	
TI	CDCVF310 T	Clock Buffer tpd	2.8	ns	
	Delay 1	1" Trace + Clk Skew	0.7	ns	
	Delay 2	2" Trace + Clk Skew	0.8	ns	
	Delay 3	3" Trace + Clk Skew	1.0	ns	
	Delay 6	6" Trace + Clk Skew	1.5	ns	
	FET ADDR AC	FET Adder A to C	6.5	ns	
	FET ADDR AS	FET Adder A to S	5.9	ns	Same as A to C but remove final Swi
	FET ADDR NC	FET Adder Nibble A to C	3.6	ns	
	FET ADDR NS	FET Adder Nibble A to S	2.9	ns	
	FET INC AY	FET Incrementer	6.4	ns	
GSI	GS84036CGT-150E	EXECUTE RAM - Enable	3.8	ns	EXECUTE RAM
GSI	GS84036CGT-150S	EXECUTE RAM - Setup tim	1.5	ns	
GSI	GS84036CGT-150T	EXECUTE RAM - CP to Q	7.5	ns	
	GS8640Z18GT-250E	EXTERNAL RAM - Enable	??	ns	EXTERNAL RAM

	GS8640Z18GT-250S	EXTERNAL RAM - Setup ti	1.5 ns	
	GS8640Z18GT-250T	EXTERNAL RAM - CP to Q	6.5 ns	
GSI	GS880Z36CGT-300E	DECODE RAM - Enable	2.5 ns	DECODE RAM
GSI	GS880Z36CGT-300S	DECODE RAM - Setup time	1.4 ns	
GSI	GS880Z36CGT-300T	DECODE RAM - CP to Q	5.0 ns	
Fairchild	NC7SV00	NAND - tpd	1.0 ns	
Fairchild	NC7SV02	NOR - tpd	1.0 ns	
Fairchild	NC7SV04	NOT - tpd	1.0 ns	
Fairchild	NC7SV08	AND - tdp	1.0 ns	
Fairchild	NC7SV32	OR - tpd	1.0 ns	
Fairchild	NC7SV74 S	Flip-Flop – Setup	1.0 ns	
Fairchild	NC7SV74 T	Flip-Flop – Clk to Q	1.0 ns	
Fairchild	NC7SV86 T	XOR - tpd	1.0 ns	

Reset Q Counter

	Component	Description	Tpd
MIR	74AVC16374 T	Register - CLK to Q	1.3
END.MX	74LVC138 S	Decoder - A to Y	2.7
Q.RESET	74CBTLV3257	MUX - Sel to Y	2.0
EXECUTE RAM	GS84036CGT-150S	EXECUTE RAM - Setup tim	1.5
			7.5

FetchMicrocode

MIR := RAM[OP, Q]	Component	Description	Tpd
EXECUTE RAM	GS84036CGT-150T	EXECUTE RAM - CP to Q	7.5
FetchOpcode.SW	NC7SV08	AND - tdp	1.0
MIR	74AVC16374 S	Register - Setup	0.0
			8.5

DECODE (uCODE)

ADH := REG.EN	Component	Description	Tpd
MIR	74AVC16374 T	Register - CLK to Q	1.3
ADH.MX	74LVC138 S	Decoder - A to Y	2.7
CC:	74AUC2G53 S	Fet Switch - Select	1.1
CC:	74AUC2G53 T	Fet Switch - Data to Y	0.1
CC:	74AUC2G53 T	Fet Switch - Data to Y	0.1
DECODE.SW	74CBTLV3257 D	MUX - Data to Y	0.3
REG.EN->FF.ADH	74AVC16374 E	Register - Enable	2.0
ADH Setup	GS8640Z18GT-250S	EXTERNAL RAM - Setup ti	1.5
			9.0

DECODE (OP)

ADH := REG.EN	Component	Description	Tpd
DECODE RAM	GS880Z36CGT-300T	DECODE RAM - CP to Q	5.0
DECODE.SW	74CBTLV3257 D	MUX - Data to Y	0.3
REG.EN->ADH	74AVC16374 E	Register - Enable	2.0
ADH Setup	GS8640Z18GT-250S	EXTERNAL RAM - Setup ti	1.5
			8.8

DECODE (OP) ALUC

ADH := REG.EN	Component	Description	Tpd
DECODE RAM	GS880Z36CGT-300T	DECODE RAM - CP to Q	5.0
ALUC.MX	74AUC2G53 S	Fet Switch - Select	1.1
ALUC.MX	74CBTLV3257 D	MUX - Data to Y	0.3
ALUC	74AVC16374 S	Register - Setup	0.0
			6.3

ResetIR

	Component	Description	Tpd
MIR	74AVC16374 T	Register - CLK to Q	1.3
END.MX	74LVC138 S	Decoder - A to Y	2.7
SYNC/INT.DETECT	NC7SV32	OR - tpd	1.0
ResetIR.SW	74CBTLV3257 S	MUX - Sel to Y	3.2
IR Setup	74AVC16374 S	Register - Setup	0.0
			8.2

ALU (ADDRESS)

ADL := ALU(ADD)	Component	Description	Tpd
ALUB	74AVC16374 T	Register - CLK to Q	1.3
FET ADDR	FET ADDR AS	FET Adder A to S	5.9
ALUR.ADD	74CBTLV3245 T	Buffer - tpd	0.3
ALUR.ADD->ADH	74CBTLV3245 T	Buffer - tpd	0.3

ADH Setup	GS8640Z18GT-250S	EXTERNAL RAM - Setup ti	1.5
			9.2

ALU (DATA)

A := ALU(ADD)	Component	Description	Tpd
ALUB	74AVC16374 T	Register - CLK to Q	1.3
FET ADDR	FET ADDR AS	FET Adder A to S	5.9
ADDR.ALU	74CBTLV3245 T	Buffer - tpd	0.3
R.RF	74CBTLV3245 T	Buffer - tpd	0.3
ALUA Setup	74AVC16374 S	Register - Setup	0.0
			7.7

BCD (WAIT)

A := ALU(op)	Component	Description	Tpd
MIR	74AVC16374 T	Register - CLK to Q	1.3
ALU.MX	74LVC138 S	Decoder - A to Y	2.7
BCD	NC7SV02	NOR - tpd	1.0
WAIT	NC7SV56	OR - tpd	1.0
WAIT	NC7SV08	AND - tdp	1.0
RDY	NC7SV74 S	Flip-Flop – Setup	1.0
			8.0

4-bit.ALU

A := ALU(op)	Component	Description	Tpd
MIR	74AVC16374 T	Register - CLK to Q	1.3
4-Bit.ALU	NC7SV00	NAND - tpd	1.0
4-Bit.ALU	74AUC2G53 S	Fet Switch - Select	1.1
			3.4
			3.6 <-- Must be < 1/2 FET Adder tp

ALU (BCD1)

A := ALU(op)	Component	Description	Tpd
ALUA	74AVC16374 T	Register - CLK to Q	1.3
Nibble Adder	FET ADDR NS	FET Adder Nibble A to S	2.9
BCD.DET.LO	74CBTLV3251 S	MUX - Sel to Y	2.8
BCD.SEL.LO	74CBTLV3257 D	MUX - Data to Y	0.3
BCD.ALUB	74CBTLV3245 T	Buffer - tpd	0.3
ALUB	74AVC16374 S	Register - Setup	0.0
			7.5

ALU (BCD2)

A := ALU(op)	Component	Description	Tpd
ALUA	74AVC16374 T	Register - CLK to Q	1.3
BCD.DET.HI.AUX	74CBTLV3253 S	MUX - Sel to Y	2.0
BCD.SEL.HI	74AUC2G53 T	Fet Switch - Data to Y	0.1
BCD.SEL.HI	74AUC2G53 T	Fet Switch - Data to Y	0.1
Nibble Adder	FET ADDR NS	FET Adder Nibble A to S	2.9
ADDR.ALU	74CBTLV3245 T	Buffer - tpd	0.3
BCD.RF	74CBTLV3245 T	Buffer - tpd	0.3
RF	74AVC16374 S	Register - Setup	0.0
			6.9

Carry Recirculate

ALUin(x, x, C.OUT)	Component	Description	Tpd
ALUC	74AVC16374 T	Register - CLK to Q	1.3
Adder	FET ADDR AC	FET Adder A to C	6.5
Cout.MX	74CBTLV3251 D	MUX - Data to Y	0.3
ALUC.MX	74CBTLV3257 D	MUX - Data to Y	0.3

ALUC	74AVC16374 S	Register - Setup	0.0
			8.3

Evaluate Flags (Implied)

P := FLAGS(ALUR)	Component	Description	Tpd	
ALUR	74AVC16374 T	Register - CLK to Q	1.3	
FLAGS		**Flags Logic**	**3.1**	
P RegisterWrite Setup	74AVC16374 S	Register - Setup	0.0	
1/2 Cycle			4.4	<– P Register clocked on PHI2
Implied Cycle			8.8	

DECODE (uCODE) FLG.MX

FTM := DECODE	Component	Description	Tpd
MIR	74AVC16374 T	Register - CLK to Q	1.3
FLG.MX	74LVC138 S	Decoder - A to Y	2.7
FLG.MX	74AUC32	OR - tdp	0.9
FLG.MX	74AUC08	AND - tdp	0.9
FLG.MX	74AUC08	AND - tdp	0.9
FTM	74AVC16374 S	Register - Setup	0.0
			6.7

BranchTest (Implied)

P := FLAGS(ALUR)	Component	Description	Tpd
IR	74AVC16374 T	Register - CLK to Q	1.3
BranchTest	74AUC2G53 S	Fet Switch - Select	1.1
BranchTest	74AUC2G53 T	Fet Switch - Data to Y	0.1
BranchTest	74AUC2G53 T	Fet Switch - Data to Y	0.1
EXIT.BTF	74AUC2G53 T	Fet Switch - Data to Y	0.1
Buffer	74AUC08	AND - tdp	0.9
FetchOpcode.SW	74AUC08	AND - tdp	0.9
Half-cycle			4.5
Implied Cycle			8.9

Exit Carry Clear (EXIT.CC)

	Component	Description	Tpd
ALUB	74AVC16374 T	Register - CLK to Q	1.3
BCD.SEL.HI	74CBTLV3253 D	MUX - Data to Y	0.3
FET Adder	FET ADDR AC	FET Adder A to C	6.5
BranchExit	74CBTLV3253 D	MUX - Data to Y	0.3
EXIT.BTF	74AUC2G53 T	Fet Switch - Data to Y	0.1
FetchOpcode.SW	74AUC08	AND - tdp	0.9
			9.3

FLAGS

	Component	Desc	Tpd	
V Select	74CBTLV3251 S	MUX - Sel to Y	2.8	
			2.8	
Z Flag Evaluate	NC7SV02	NOR - tpd	1.0	– 8 Signals –> 4
	NC7SV08	AND - tdp	1.0	– 4 Signals –> 2
	NC7SV08	AND - tdp	1.0	– 2 Signals –> 1
Z Select	74AUC2G53 T	Fet Switch - Data to Y	0.1	
			3.1	
N Select	74AUC2G53 S	Fet Switch - Select	1.1	

Max Flag			3.1

Repeat Carry Set

	Component	Description	Tpd	
MIR	74AVC16374 T	Register - CLK to Q	1.3	
END.MX	74LVC138 S	Decoder - A to Y	2.7	
Repeat	74AUC04	NOT - tpd	0.3	
Repeat	NC7SV00	NAND - tpd	1.0	
Q Counter	74LVC161 S	Counter - Setup	2.5	
			6.5	

Incrementer 16-Bit

	Component	Description	Tpd	
ADL/ADH	74AVC16374 T	Register - CLK to Q	1.3	
INC16	FET INC AY	FET Incrementer	6.4	
INC.ADH	74CBTLV3245 T	Buffer - tpd	0.3	
ADL/ADH	74AVC16374 S	Register - Setup	0.0	
			8.0	

Synch Read

ALUB := MEM(ADL/ADH)	Component	Description	Tpd	
External Memory	GS8640Z18GT-250T	EXTERNAL RAM - CP to Q	6.5	<– /OE controlled by address decoding
D -> ADH	74CBTLV3245 T	Buffer - tpd	0.3	RC (5Ω * 5pF * 5ICs) = 250ps
ADH Setup	GS8640Z18GT-250S	EXTERNAL RAM - Setup ti	1.5	<–!D -> DB Invert Operand for ALUB pat
			8.3	

Synch Read Inverted

ALUB := MEM(ADL/ADH)	Component	Description	Tpd	
External Memory	GS8640Z18GT-250T	EXTERNAL RAM - CP to Q	6.5	<– /OE controlled by address decoding
Inverter	74AUC1G86	XOR - tdp	0.8	
D -> ADH	74CBTLV3245 T	Buffer - tpd	0.3	RC (5Ω * 5pF * 5ICs) = 250ps
ALUB Setup	74AVC16374 S	Register - Setup	0.0	<–!D -> DB Invert Operand for ALUB pat
			7.6	

Asynch Read (Wait-State)

ADH := MEM(ADL/ADH)	Component	Description	Tpd	
ADL/ADH	74AVC16374 T	Register - CLK to Q	1.3	
ABL/ABH	74CBTLV3245 T	Buffer - tpd	0.5	<– (6.2Ω * 5pF * 16) = 500ps
Peripheral			**10.0**	
DB -> D	74CBTLV3245 T	Buffer - tpd	0.3	<– Elmore delay
D -> ADH	74CBTLV3245 T	Buffer - tpd	0.3	<– RC (5Ω * 5pF * 5ICs) = 250ps
ADH Setup	GS8640Z18GT-250S	EXTERNAL RAM - Setup ti	1.5	<–!D -> DB Invert Operand for ALUB pat
2-Cycle			13.8	
Implied Cycle			6.9	

Asynch Write (Wait-State)

MEM(ADL/ADH) := A	Component	Description	Tpd	
ADL/ADH	74AVC16374 T	Register - CLK to Q	1.3	
ABL/ABH	74CBTLV3245 T	Buffer - tpd	0.5	<– (6.2Ω * 5pF * 16) = 500ps
Peripheral			**10.0**	
2-Cycle			11.8	
Implied Cycle			5.9	

6510 Port Read

ADH := MEM(6510)	Component	Description	Tpd

ADL/ADH	74AVC16374	T	Register - CLK to Q	1.3
PB.CS	74AUC02		NOR - tpd	0.9 24 -- 12
PB.CS	74AUC08		AND - tdp	0.9 12 --> 6
PB.CS	74AUC08		AND - tdp	0.9 6 --> 3
PB.CS	74AUC08		AND - tdp	0.9 3 --> 2
PBAD	74AUC2G53	S	Fet Switch - Select	1.1
PBAD	74AUC2G53	T	Fet Switch - Data to Y	0.1
PBAD	74AUC2G53	T	Fet Switch - Data to Y	0.1
PDR -> D	74AVC16374	E	Register - Enable	2.0
D -> ADH	74CBTLV3245	T	Buffer - tpd	0.3
ADH Setup	GS8640Z18GT-250S		EXTERNAL RAM - Setup ti	1.5
				9.9

6510 Port Write

MEM(6510) := A	Component		Description	Tpd
ADL/ADH Bus	74AVC16374	T	Register - CLK to Q	1.3
PB.CS	74AUC02		NOR - tpd	0.9 24 -- 12
PB.CS	74AUC02		NOR - tpd	0.9 12 --> 6
PB.CS	74AUC08		AND - tdp	0.9 6 --> 3
PB.CS	74AUC08		AND - tdp	0.9 3 --> 2
PB.CS	74AUC08		AND - tdp	0.9 2--> 1
Write Enable	74AUC08		AND - tdp	0.9
Write Enable	74AUC08		AND - tdp	0.9 – A0, R/W, PB.CS
	74LVC138	E	Decoder - Enable	2.9
POD	74AVC16374	S	Register - Setup	0.0
				10.5