MEMWR is not qualified by the ROM chip select to allow writing to ram underneath the ROM.

ROM select and wait state

RDY source selector

I/O read/write generation

I/O Wait states

Interrupt request logic
X4,X5 driven by addressable latch external to this circuit

The vector pull operation in native mode accesses a pair of registers. The low order address bits are determined by the interrupt request level, spaced 4 bytes apart. The high order address bits come from a programmable latch. This allows any 64 byte region in the lower 64k bank to be selected as a vector target.

The VPB4 signal feeds into the ROM chip select logic to disable the ROM during a native mode vector fetch.

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