EDN μP DESIGN SERIES

2-1/2-generation μP's—$10 parts that perform like low-end mini's

Experience with first- and second-generation μP's has produced a round of MOS units fine-tuned to deliver most performance/dollar.

Robert H. Cushman, Special Features Editor

A class of what might be called 2-1/2-generation microprocessors is now entering the marketplace. This includes the MOS Technology 650X family, the National SCAMP and the Electronic Arrays 9002. These machines tend to cut corners to keep chip manufacturing costs down, but not in ways that will hurt the performance for most main-stream applications. In fact some of these new 2-1/2-generation μP's will outperform the popular Intel 8080 and Motorola 6800 second-generation devices on simple benchmarks.

We estimate that the parts cost of these μP's and their associated support chips will drop to $10 sometime in 1976. This means the LSI parts kits for low-end μP systems will drop to the $20-$30 range in 1976, as only two or three chips will be needed to make up complete μP systems.

These 2-1/2-G μP's have been intentionally designed to meet this low level of end-product price goals. They typically include either wholly or partially built-in clocks, built-in I/O ports, built-in RAM or combined ROM/RAM chips, and simple, low-drain power supply requirements. Complete, functional μP subsystems—mounted on pc boards, and with power supplies—should be possible under $50. These minimal systems will have 1000 to 2000 bytes of ROM, about 100 bytes of RAM, and perhaps four I/O ports.

We will analyze these 2-1/2-G machines in this and following articles. In addition to the brand new μP's named above, we'll be re-evaluating some of the second-generation machines in light of the changing competitive situation.

Who's who and what's what

The Fairchild F-8 certainly must be considered as strong continuing competition, for it also represents low minimum-system parts cost. Likewise the "face-lifted" versions of those last-generation earlybirds, the Intel 4004 (facelifted to the 4040), the Rockwell PPS-4 (facelifted to the PPS-4/2) and National IMP-16 (facelifted to the PACE) must be considered.

We won't be forgetting the 2nd-generation machines like the Intel 8080, Motorola 6800, Rockwell PPS-8, and Signetics 2650. With μP's you can never safely assume that any supplier has stopped cranking in improvements. On the contrary, there is such a heavy investment in these parts and their associated support chips that you can bet that the manufacturer is constantly re-designing his masks and tweaking his manufacturing line to get increased part speed and lowered cost. From reports we've heard from various manufacturers, we gather that any given μP can be made to run 50% to 100% faster than its initial specs. Additionally, its chip can be redesigned for at least a 25% size reduction. As we have said in the past, μP's represent constantly moving targets with 10-year potential lifetimes.

We will not consider either the CMOS μP's or the bipolar bit-slice ones, as these have no hope of reaching down to the "dirt cheap" prices of single-channel, single-chip MOS μP's during 1976. (Who knows what will happen by 1977?)

A stripped-down 6800

The first 2-1/2-G μP that we've obtained parts for is the MOS Technology 650X family. National's SCAMP—a PMOS part—also exists we've been told. Electronic Arrays' 9002 is in mask preparation and first parts are expected in October.

The MOS Technology 650X family represents a conscious attempt of eight former Motorola employees who worked on the development of the 6800 system to put out a part that would replace and outperform the 6800, yet undersell it. With the benefit of hindsight gained on the 6800 project, the MOS Technology team headed by Chuck Peddle, made the following architectural changes in the Motorola CPU:

- The second "B" accumulator was omitted.
- Two bytes of the 6800 single index register "X" were split into two "X" and "Y" index registers that are each one byte long. At the same time the controls were altered so that

these shorter indexes would operate in the "true" indexing mode.

- Three-state control was eliminated from the address bus outputs.
- The clock was included on the chip.
- Control bus signals were simplified, eliminating the need for a VMA (valid-memory address) output and adding an "8080-type" RDY signal for single-cycle stepping.
- Some register resets were dropped from the initializations routine (evoked by the RESET line as on the 6800).

Fig. 1 shows the resulting architecture of the 6502 version of the 650X family. This can be

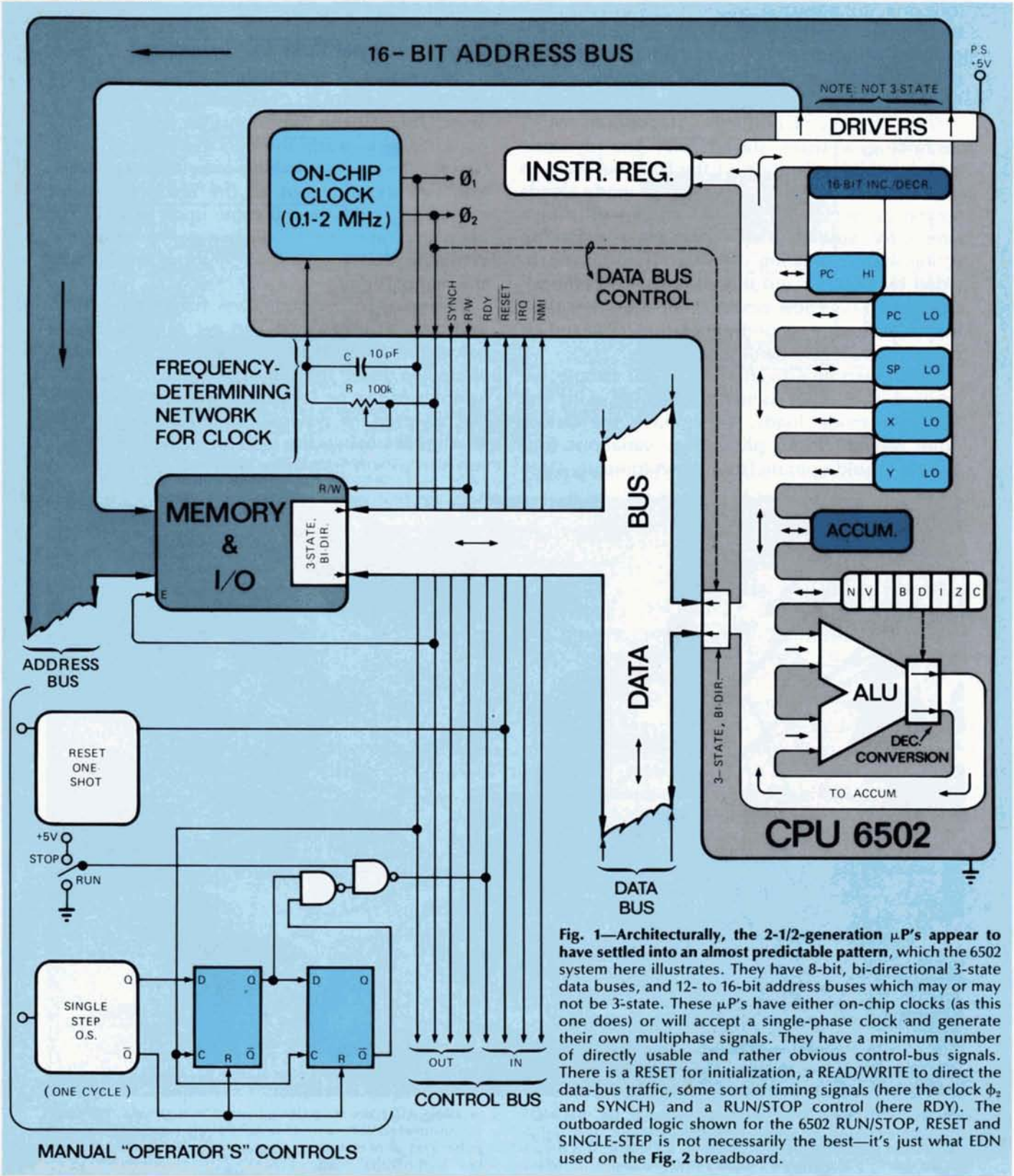

Fig. 1—Architecturally, the 2-1/2-generation μP's appear to have settled into an almost predictable pattern, which the 6502 system here illustrates. They have 8-bit, bi-directional 3-state data buses, and 12- to 16-bit address buses which may or may not be 3-state. These μP's have either on-chip clocks (as this one does) or will accept a single-phase clock and generate their own multiphase signals. They have a minimum number of directly usable and rather obvious control-bus signals. There is a RESET for initialization, a READ/WRITE to direct the data-bus traffic, some sort of timing signals (here the clock ϕ_2 and SYNCH) and a RUN/STOP control (here RDY). The outboarded logic shown for the 6502 RUN/STOP, RESET and SINGLE-STEP is not necessarily the best—it's just what EDN used on the **Fig. 2** breadboard.

compared to the similar drawing EDN did for the 6800 in **Fig. 2** of **Ref. 1**. An understanding of what MOS Technology means by saying that their index registers have "true" indexing can be obtained by comparing the indexing of the Signetics 2650 in **Ref. 2** with that of the 6800 in the same reference. The Signetics μP also has true indexing, for the base address is carried in the instruction and the offset is added by the index register. Motorola's 6800 puts the base address in the index register and lets the instruction carry the offset.

From the semiconductor standpoint, MOS Technology's team stayed with the dynamic 2-phase clock operation of the 6800 but went to depletion-mode loads. Depletion-mode loads appear to be especially helpful to devices using a single 5V supply. They give good switching action—approximating the sharp transitions provided by CMOS—and this, in turn, allows the μP circuitry to have low power dissipation (less than half that of some second-generation μP's) and be driven more easily by on-chip clocks.

In our own investigations of a 6502 sample, we verified two other benefits obtained with the depletion-mode loads. They make the device quite tolerant to supply voltage variations (our sample would operate from down to nearly 4V to over 6V) and were able to operate with a wide range of clock speeds on each side of the nominal 1-MHz target (we could adjust the clock of our sample from less than 100 kHz to over 2 MHz). Additionally, the circuit appeared to have good noise immunity. This, if true, might be a by-product of the quasi-CMOS switching given by depletion-mode loads.

Quick and painless to "bring up"

Newcomers to μP's will find these 2-1/2-G μP's much less painful to "get going" than previous ones. This can be important, we think, for the easiest way to wade through the support literature for these μP's is to have one running at hand. You can then try out all the instructions and operating modes as you come upon them in the manuals. Time and time again we've found the actual device explains itself far more lucidly than the manuals do.

The 6502, for example, was hardly more time and trouble to wire up and get running than a calculator chip. **Fig. 2** shows the breadboard setup we used for our first tests of the 6502 sample. As can be seen there was not much to it. We powered the system off a series string of four #6 dry cells (while the cells were fresh we could run the μP off just three of them). The on-chip

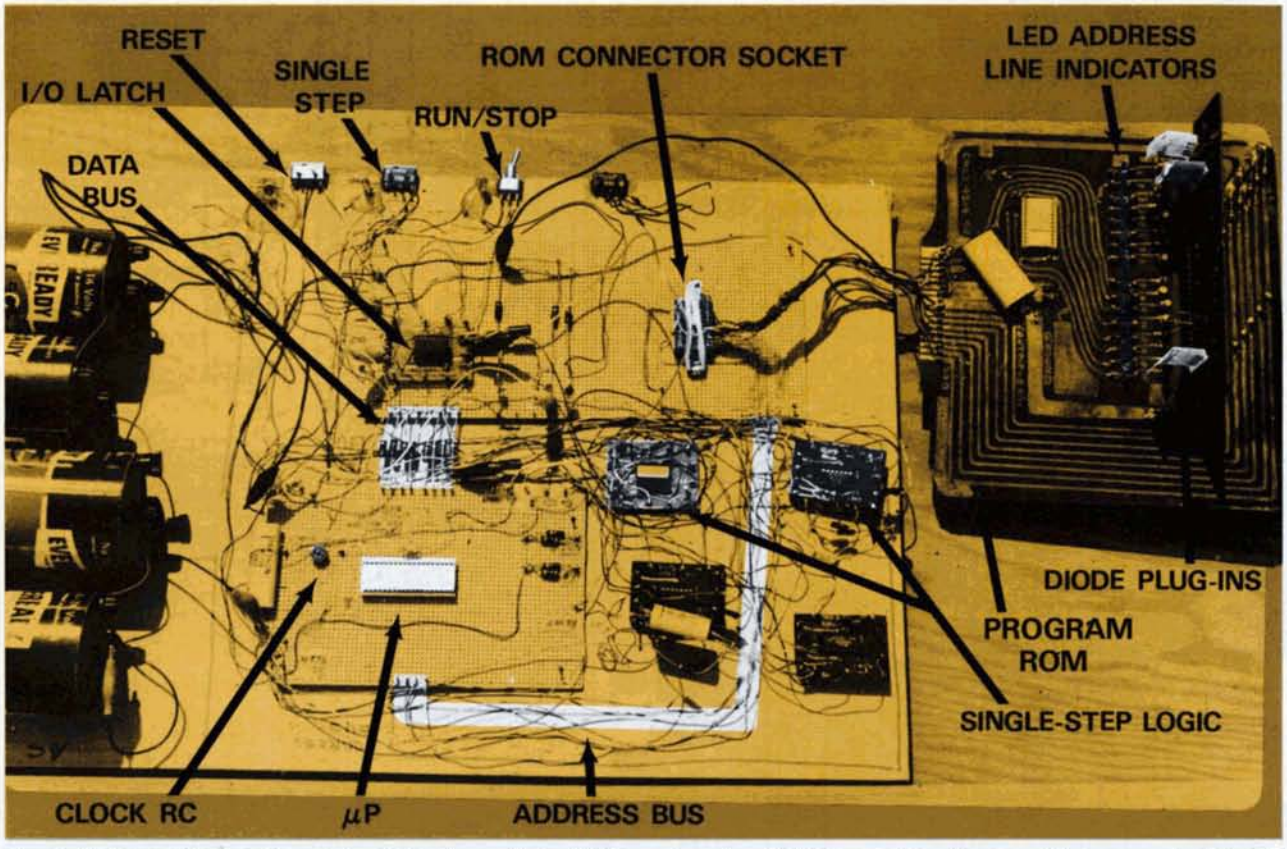

Fig. 2—EDN's initial breadboard for "bringing up" the MOS Technology 6502 μP illustrates how simple the 2-1/2-generation machines are hardwarewise for users. This breadboard was laid out (inside a week's time) to approximate the topology EDN has used to diagram μP's in general. Although we discovered quite a bit of noise (mostly coupling in of clock pulses) on all of our rather long and spread-out lines, the 6502 operated without malfunction.

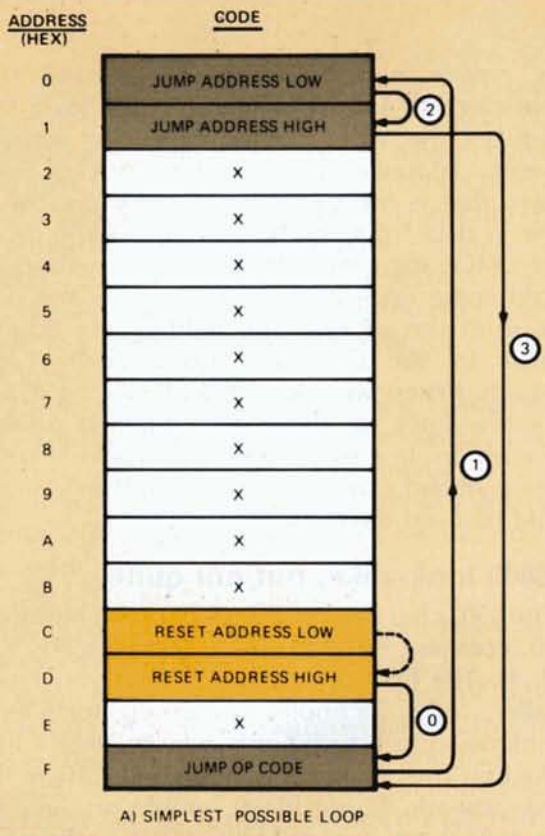

Fig. 3—These elementary programs show how to put the 6502 into loops so that scope signals can be generated in RUN mode or a repeating sequence of behavior can be observed in single-step mode. Program (**a**) represents a bare minimum loop while program (**b**) incorporates a read (LDA, Immediate) and a write (STA accumulator) operation. If the nonmaskable interrupt $\overline{\text{NMI}}$ line is grounded during singlestepping through program (**b**), the PC points to ROM lines A and B and then jumps to the address specified by code in A and B. Rod Orgill of MOS Technology says this program happens to contain the worst case timing for the μP as it asks the PC (program counter) to generate all carries when going from FFFF to 0000.

clock oscillator would oscillate without any help once power was applied to the chip, but to control the frequency we used a single 15-pF capacitor and a 100k pot. CMOS gates and D-type FF's were used for the RESET and SINGLE-STEP logic. The manual controls for these inputs can be seen expoxied along the front edge of the board.

Tune in the program and run

For our program, we used the 16-line ROM described in **Ref. 3**. We plugged in the diode assemblies to generate the elementary programs shown in **Fig. 3**. The 6502 goes through a type of RESET start-up routine that is used by a number of μP's. When the RESET line is pulled low, a hardwired JUMP op code is fetched, with the two address bytes being automatically taken from memory locations hex FFFC and FFFD. We merely left out the diodes in these C and D locations in our ROM (**Fig. 3**) so that the address FF was in both C and D. (Our ROM had negative logic where the absence of a diode would produce a ONE for the 6502.)

This jumped the 6502's PC (program counter) so that it fetched the first instruction of the program from the last line, F, of the ROM, an action that could be visually seen by the glow on the LED in the circuit driving the last line. In our first program (as in **Fig. 3**), we plugged the op code for the 6502's JUMP instruction in line F. The 6502's JUMP is a 3-byte instruction, so the PC would increment and continue on, looking for the remaining two address bytes. It would "wrap around" to ROM location "0" (actually hex 0000 in the full 16-bit address space). Here again, we didn't bother to insert any diodes. Thus, the address for this jump was again FFFF, and the program jumped back to itself at line F, putting the 6502 into a tight little loop. This looping was easy to verify visually, because the LED's on the ROM address drive lines only glowed at location 0, 1 and F.

With the 6502 in this tight loop we examined the signal waveforms on all bus lines. A fair amount of noise existed on the signals because of our sloppy wiring on this initial breadboard, but in spite of this, there was no evidence of any malfunctioning.

We simulated the effect of larger memories by adding capacitance on the lines. We discovered that at moderate 500-kHz clock speeds, the 6502 could drive capacitive loads as large as 10,000 pF on the address lines. Our tests were not conclusive, of course, because they were done just at room temperature, but they did appear to indi-

cate that this 2-1/2-G μP should be able to drive fairly large memories without the help of buffers.

One step at a time saves...

When the 6502 was put into the STOP mode and single stepped, the ROM address LED indicators would glow one after the other as the SINGLE-STEP button was pushed. We found this single-cycle step mode quite handy for tracing the executions of multibyte instructions. It gives one a chance to leisurely examine the logic levels on all the bus lines at each stage of the execution.

Next, we plugged in the slightly more elaborate program shown in **Fig. 3b**. This had a "load accumulator immediate" instruction (LDA) and a "store accumulator" (STA). Therefore we could observe the 6502 in both a read and a write mode. Again, a JUMP FFFF was put in to lock the 6502 into a convenient repeating loop. We learned two things about the 6502 when observing its behavior in this loop. First, when single stepping, the machine would not stop on a write cycle, but would race through at regular speed to stop on the next read cycle. This is normal behavior with the 6502 and is described in the data sheets. It's shown as step 4 in **Fig. 3**.

Second, we found that the concept of the "6800 bus," which the 6502 adheres to, demands that there can't be too much delay in the logic that produces the write strobe signal for external devices. Supposedly when the clock ϕ_2 goes down, that is the signal for external devices to latch in data from the bus during a write cycle. Our CMOS logic had rather long delays and we noted some uncertainty as to whether the data bus from the μP was still holding the correct signals by the time the strobe finally came through. When we added 100 pF loading to the data bus lines for delay, we obtained reliable write action. In a real system you would hope to have matched components so that the ϕ_2 signal could be used directly.

A 6800 look-alike, but not quite

The 6502 chip physically looks like the Motorola 6800 (compare **Fig. 4** in this article with **Fig. 1** in **Ref. 1**). The final target size is, however, much smaller. MOS Technology is aiming for a final shrink down to 153×168 mils, which will be a 10% reduction over the current oversized runs of the mask artwork during initial sample production. The 650X team had to help MOS Technology bring up an n-channel line for this processor, but, according to Terry Holdt, that line is now

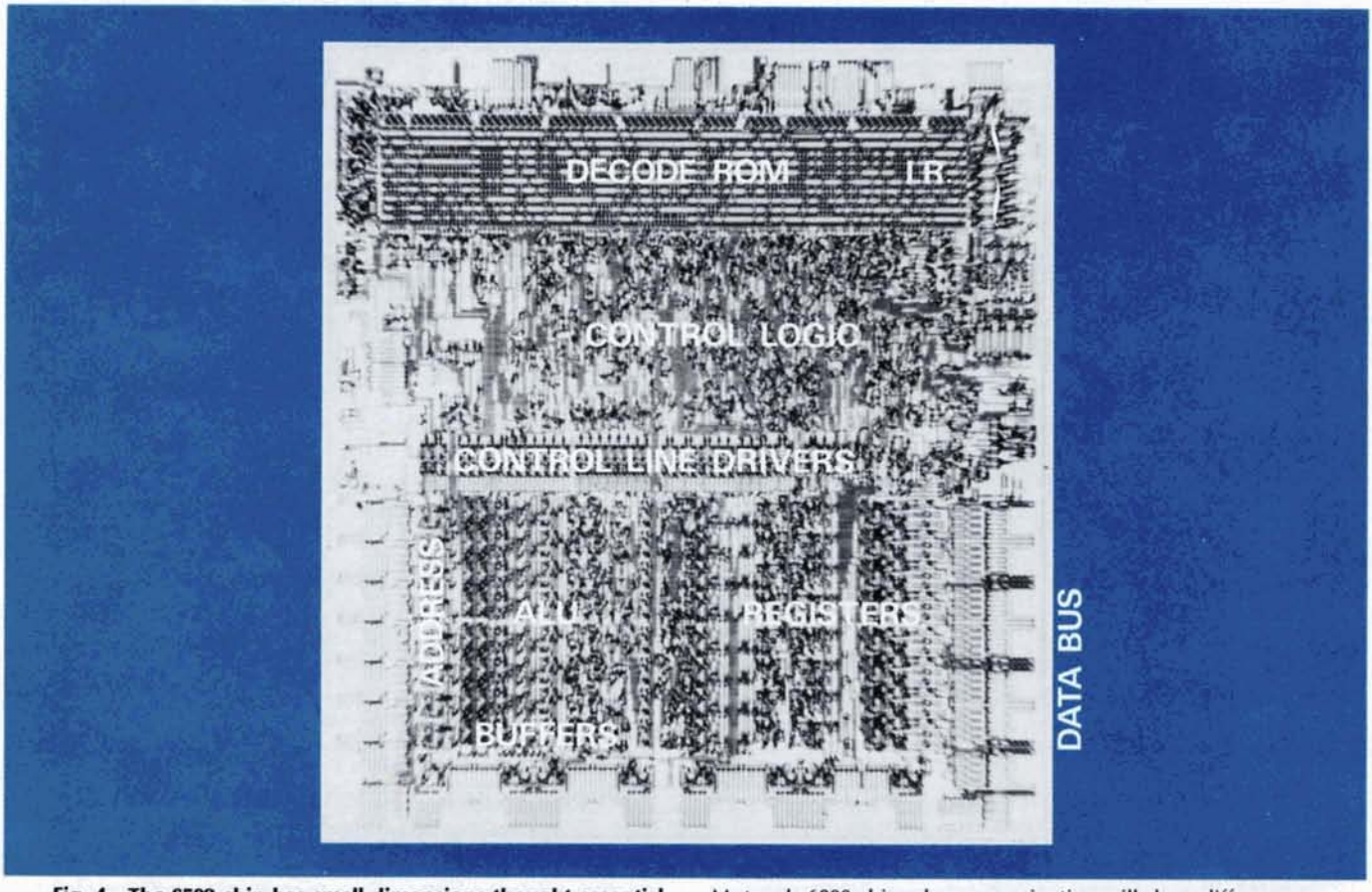

Fig. 4—The 6502 chip has small dimensions thought essential for really low-cost n-channel silicon-gate products. It measures just 168×183 mils now and will be shrunk 10% to 153×168 mils soon. While at first glance it appears identical to the Motorola 6800 chip, closer examination will show differences, some of which are enumerated in the text. The clock oscillator is along the upper edge above the ROM that decodes the instruction register.

operational and will be processing 3-in. wafers soon (if not by the time this article appears).

Internally, quite a few changes have occured in the 650X family chips, according to Rod Orgill and Will Mathys of the design team. They conserved on-chip real estate by eliminating some of the 6800's registers. In addition omitting the extra accumulator and the top half of the stack pointer (SP), the designers dropped some of the 6800's temporary registers.

The most visually obvious space saving was at the address output buffers. Eliminating these 3-state devices allowed MOS Technology to shrink the buffer size considerably. Peddle's advice to those users who feel they must be able to float the address bus for DMA "take-overs" is to hang a TTL 74158 MUX on the address bus. "For the large, fast systems that would want DMA, you'll need a TTL buffer anyway," he said.

Space was saved in the 650X's control logic by including only 55 of Motorola's 72 instructions. MOS Technology left out six of the 6800's rich repertoire of PDP-11 branch instructions and the half dozen or so instructions that the 6800 used to manipulate data between its two accumulators. Peddle claims the new μP still has more than enough branch instructions. Moreover, the machine obviously can't use any two-accumulator instructions since it has only one accumulator.

Room for growth

Apparently the design team had another reason beyond saving chip space that prompted them to cut out instructions. They wanted to keep open op-code bit patterns for future "growth" versions of the first baseline models. Peddle has planned the 650X product line after the upward-compatible growth concepts that have been used so successfully by large computer manufacturers.

Thus, MOS Technology has left holes in the 650X instruction bit pattern to accommodate a "quasi-16-bit machine."

According to Peddle, his architecture more than compensates for the missing instructions by having better addressing options for the remaining instructions. "Fancy instructions are often only an attempt to make up for bad addressing," he says. The 6502's superior performance on the AH Systems benchmarks (winning four out of five of them over the 8080 and 6800) would, if accurate, indicate that his shift in emphasis to improved addressing has worked.

With all their paring down of 6800 architecture, MOS Technology designers still managed to squeeze some features onto the chip that the 6800 doesn't have. They added a decimal conversion unit at the output of the ALU. A decimal-mode bit in the status register, when set, activates this conversion unit and gives the 650X family genuine decimal capability without the programmer having to remember to throw in "decimal adjusts." Decimal operation will also be a built-in software-evoked optional operating feature of the EA9002.

As compared to the other low-cost 2-1/2-G machines, the 6502 appears to have one possible drawback in minimum-component systems. All 650X CPU's must have external RAM to implement the off-chip subroutine and interrupt save stacks to make up for the single accumulator in the CPU. In contrast, Electronic Arrays' 9002 has a 7-level internal push-down stack for its PC subroutine nesting and 64 bytes of internal RAM. Therefore, the 9002 can get by without any external RAM.

To accommodate this need for external RAM, MOS Technology is working on a combined ROM/RAM chip. This will be a very ambitious, large n-channel chip (present dimensions are 229×208 mils). However, this "6530" will contain "everything but the kitchen sink." It will have 1k bytes of ROM, 64 bytes of RAM, 16 pins of sophisticated I/O, and a built-in timer. With this all-inclusive 6530 support chip, Peddle believes the 650X family will have the most economical 2-chip system on the market.

Watch the moving targets

What do the 2-1/2-generation machines mean to older second-generation machines? "We'd probably lose a lot of business to the 6502," says Motorola's Tom Bennett, master architect of the 6800, "if we just sat still with the original 6800. But we've worked at cutting our chip size way down, plus adding many features." Bennett implied that Motorola would meet the 6502 competition with a machine that would retain all the instructions of the 6800, but add 6502 features, like depletion-mode load circuits and dual-index registers, that were thought important. He agreed that all popular μP chips will probably undergo dozens of chip redesigns during their product lifetimes, just as has been the case with the popular MOS memory chips.

In future articles in this series on 2-1/2-G machines, we will continue with our analysis of the 6502 and go on to analyze the machines from National and Electronic Arrays and any others that appear. Hopefully we'll also have a chance to look at some of the calculator chips that have been upgraded into 1-chip μP's. □

References

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2. *"Microprocessor benchmarks: How well does the μP move data?," EDN, May 20, 1975, pg. 43.*
3. *"How to get acquainted with a μP," EDN, Sept. 20, 1974, pg. 46.*